S.E. Sem. III [CMPN]

Digital Logic Design and Analysis

Prelim Question Paper

Time : 3 Hrs.] **[Marks : 80**

N.B.: (1) Question No. **1** is **compulsory**.
(2) Assume suitable data if necessary.
(2) Attempt any three questions from remaining questions.

1. (a) Implement Ex-OR gate using Four NAND gates only. **[5]**
(b) Explain TTL NAND gate. **[5]**
(c) Convert JK Flip-Flop into D Flip-Flop and T Flip-Flop. **[5]**
(d) Explain twisted ring counter. **[5]**

2. (a) State and prove De-Morgan theorem. **[10]**
(b) Reduce the following function using Quine Mc-Clusky method : **[10]**
$f(A,B,C,D) = \sum m(2,3,5,7,10,13,15)$

3. (a) Design gray to binary code converter. **[10]**
(b) Design 4 bit synchronous converter using JK Flip-Flop. **[10]**

4. (a) Explain 4 bit bidirectional shift register. **[10]**
(b) Implement following function using : **[10]**
(i) 8:1 mux, (ii) 4:1 mux, (iii) 2:1 mux
$Y = \sum m(0,1,2,3,8,9,13,14)$

5. (a) Draw neat circuit diagram and explain master slave JK flip-flop with NAND gates. **[10]**
(b) Design 3:8 decoder using basic logic gates. **[10]**

6. (a) Explain features of VHDL. **[6]**
(b) Explain BCD adder with suitable example. **[7]**
(c) Compare FPGA and CPLD. **[7]**

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