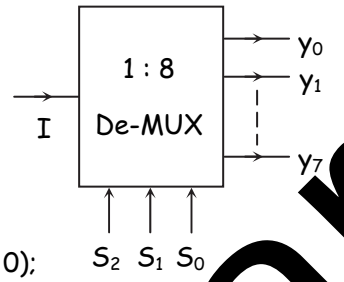
Q.6(c) Write VHDL code for De-mux. **[8]**

(A)




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity demux1_8 is
   Port ( I : IN STD_LOGIC;
        S : IN STD_LOGIC_VECTOR(2 downto 0);
        Y : OUT STD_LOGIC_VECTOR(7 downto 0));
END demux1_8;

ARCHITECTURE behavioral OF demux1_8 IS

BEGIN
PROCESS(s)
BEGIN
If (I = 1) then
CASE s IS
                WHEN "000"=>y<="00000001";
                WHEN "001"=>y<="00000010";
                WHEN "010"=>y<="00000100";
                WHEN "011"=>y<="00001000";
                WHEN "100"=>y<="00010000";
                WHEN "101"=>y<="00100000";
                WHEN "110"=>y<="01000000";
                WHEN OTHERS =>y<="10000000";
                Else y<="00000000"
END CASE;
END PROCESS;
END behavioral;
```

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