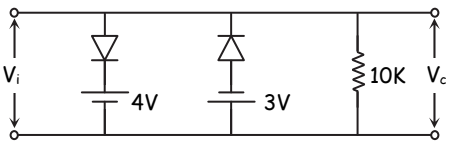
Q.1(a) Compare BJT and JFET. **[5]**

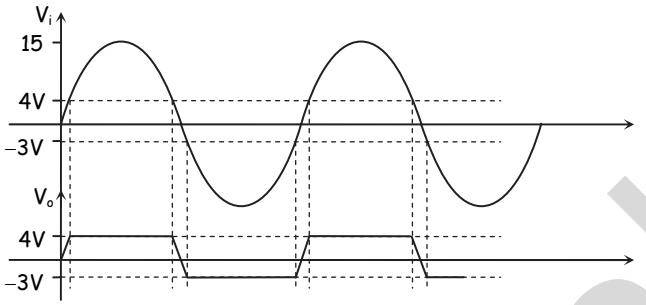
(A)

	BJT	JFET
1	BJT is a bipolar device, both majority and minority carriers take place in electrical conduction.	JFET is an unipolar device, electron current in N–channel and hole current in P–channel.
2	BJT is current operated device, it is a current controlled current source.	JFET is voltage operated device, it is a voltage controlled current source.
3	BJT has high g_m and hence provides large gain	JFET has low g_m and hence provides low gain.
4	BJT has low input resistance (Ω – kΩ) $\therefore$ input junction is forward biased.	JFET has high input resistance (MΩ) $\therefore$ input junction is reverse biased.
5	Thermal runaway is possible in BJT. $\therefore$ I_C increases when temperature increases.	Thermal runaway is not possible in JFET. $\therefore$ I_D decreases when temperature increases.
6	BJT can be operated with low values of supply voltage (3 – 10) V	JFET requires large supply voltage (> 10) V
7	BJT is noisy in operation.	JFET is less noisy in operation.
8	Requires large area while fabrication of IC's.	Requires less area while fabrication of IC's.
9	Less susceptible to damage while handling.	More susceptible to damage while handling.
10	Very complex biasing circuits required to provide stability.	Biasing circuits are less complex when compared to that of BJT.
11	Cannot be used as a voltage variable resistance	It can be used as a voltage variable resistance

Q.1(b) Obtain output for the clipper circuit shown in Figure. If a sine wave of 15 sin wt is applied as an input. Assume practical diode with suitable cut in voltage. **[5]**



(A)



Q.1(c) Write short note on small signal model of a diode. **[5]**

(A) Small–signal approximation :

- The diode is operated at a dc bias point and a small ac signal is superimposed on the dc quantities :

$$v_D(t) = V_D + v_d(t)$$

$$i_D(t) = I_s e^{v_D/nv_T} = I_s e^{v_D + v_d(t)} = I_s e^{v_n/nv_T} = I_D e^{v_n/nv_T}$$

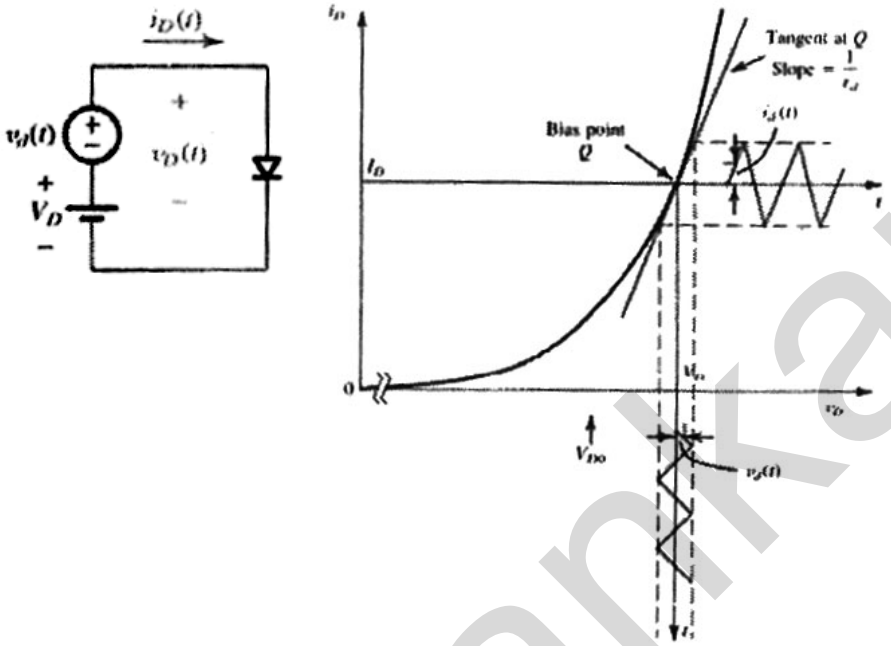
- Under small–signal condition : $v_d / nV_T << 1$

$$i_D(t) \approx I_D\left(1 + \frac{v_d}{nV_r}\right) = I_D + \frac{I_D}{nV_T} v_d = I_D + i_d$$

  - I_D associates with $V_D \rightarrow$ dc operating point Q
  - i_d associates with $v_d \rightarrow$ small signal response
- The diode exhibits linear I–V characteristics under small–signal conditions ($V_d \leq 10$ mV)
- Diode small–signal resistance and conductance at operating point Q :

$$i_d = \frac{I_D}{nV_T} v_d = g_d v_d = v_d / r_d \rightarrow g_d = \frac{I_D}{nV_T} = \left[\frac{\partial i_D}{\partial v_D}\right]_{i_D/I_D}$$

$$\rightarrow r_d = \frac{nV_T}{I_D} = I \Big/ \left[\frac{\partial i_D}{\partial v_D}\right]_{i_D/I_D}$$

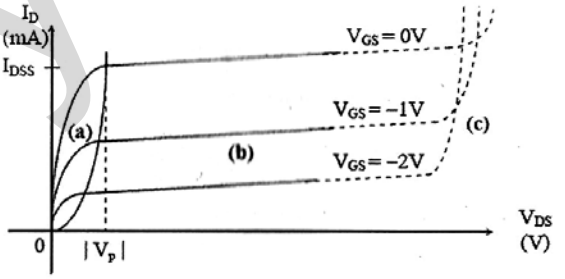


The diode small–signal model

- Choose proper dc analysis technique or model to obtain point Q
- The small–signal model is determined once Q is provided
- The small–signal model is used for circuit analysis when the diode is operating around Q

Q.1(d) Write short note on Regions of operation of FET. [5]

(A) For a given JFET I_{DSS} and V_{GS} off is a constant. The V–I characteristic of JFET is as shown.



Regions of operation of JFET

The JFET V – I characteristics is divided into three regions :

(a) Ohmic region : In this region JFET works as a Voltage Variable Resistor (VVR). For low values of V_{DS}, the drain current increases linearly with increase in V_{DS}. In this region the channel resistance remains constant for a given value of V_{GS}. When V_{GS} becomes more negative, the drain current decreases and the channel resistance increases.

(b) Pinch off region : When $V_{DS} > V_P$, the drain current I_D becomes independent of V_{DS} for a given value of V_{GS}. Also if V_{GS} changes, there is a proportional change in I_D. In this region JFET works as a Voltage Control Current Source (VCCS). Also $i_d \propto v_{gs}$, where JFET operate as an amplifier.

(c) Breakdown region : When V_{DS} becomes very high, the reverse bias across the gate channel junction increases, and it can undergo junction breakdown. The drain current increases to a very high value, if the current is not limited externally, it can cause damage to JFET. (This is due to the large field existing across the junction).

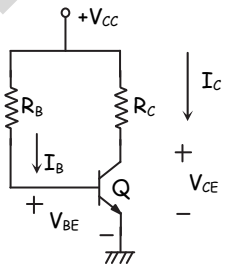
Q.2(a) Define stability factor. Derive the equation for stability factor [10] fixed base bias and emitter bias. State which biasing technique is more stable? Justify your answer.

(A) Current stability factor S_I / S

It is defined as the ratio of the change in the collector current to the change in the leakage current, keeping β and V_{BE} constant.

$$S_I = \frac{\Delta I_C}{\Delta I_{CO}}, \quad \beta, V_{BE} \text{ constant}$$

Fixed Bias: the circuit diagram ia as shown.



To find S_I, By definition,

$$S_I = \frac{\Delta I_C}{\Delta I_{CO}}, \quad \beta, V_{BE} \text{ constant}$$

$$S_I = \frac{(1+\beta)}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

For fixed bias, $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ = constant

Hence $\frac{\partial I_B}{\partial I_C} = 0$

$\therefore \quad S_I = 1 + \beta$

The value of S_I is very high. Hence poor Q point stability

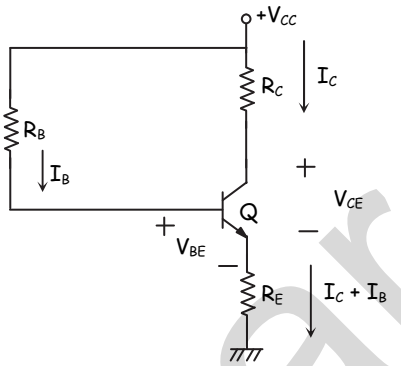
Self bias [Emitter bias]

The circuit diagram of self bias BJT is as below shown.

To find S_I

By definition, $S_I = \frac{\Delta I_C}{\Delta I_{CO}}, \beta, V_{BE}$ constant

$$S_I = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$



Apply KVL to base loop

$$V_{CC} = I_B R_B + V_{BE} + (I_C + I_B)R_E$$

$$V_{CC} - V_{BE} = I_B(R_B + R_E) + I_C R_E$$

Differentiate with respect to I_C

$$0 = \frac{\partial I_B}{\partial I_C}(R_B + R_E) + R_E$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E}$$

Negative sign shows that when I_C increases, I_B decreases and vice versa.

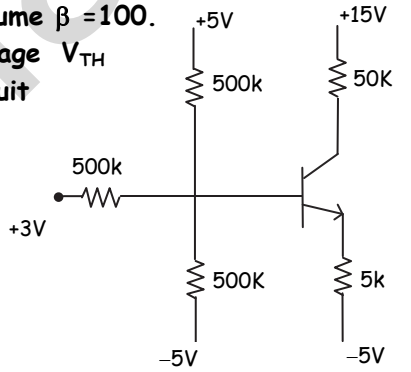
$$\therefore \quad S_I = \frac{1+\beta}{1+\beta\frac{R_e}{R_B + R_e}}$$

Sico for emitter bias is much samaller than Fixed base bias, hence Emitter bias is technique is better than Fixed base bias.

Q.2(b) For the circuit shown in Figure, assume β =100. **[10]**

(i) Find Thevenin's equivalent voltage V_{TH} and resistance R_{TH} for base circuit

(ii) Determine I_{CQ} and V_{CEQ}



(A)

$$V_{Th} = \frac{500}{(500\,||\,500)+500}[5-5+3] = 2V$$

$$R_{Th} = 500 \,||\, 500 \,||\, 500 = 166.6\ K\Omega$$

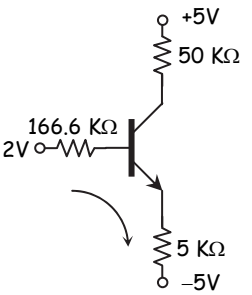
$$I_{BQ} = \frac{+5+2-V_{BE}}{166.6\,K\Omega + (1+\beta)R_E} = 9.38\ mA$$

$$I_{CQ} = \beta\, I_B = 9.38\ mA$$

$$V_{CEQ} = V_{CC} + V_{EE} - I_C\,[R_C + R_E]$$

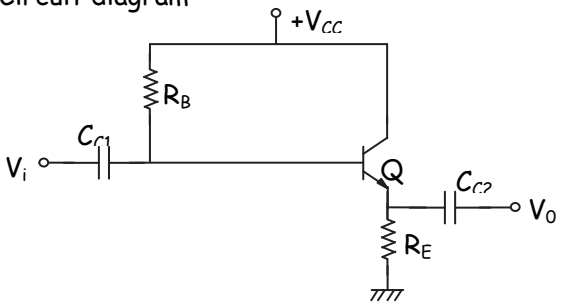
$$= 15 + 5 - 0.93\,[50 + 5]$$

$$V_{CEQ} = -31.15\ V$$



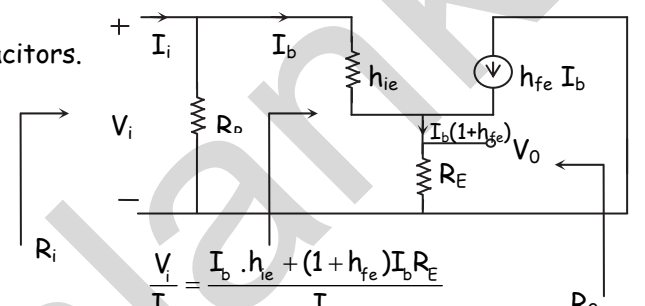
Q.3(a) Derive the equations for A_v, A_i, R_i and R_o for a Emitter Follower. [10]

(A) (a) Circuit diagram



Since output is taken from emitter, emitter voltage follows the base voltage and hence the name emitter follower.

(b) ac Equivalent circuit
Short V_{CC}, short all capacitors.



$$\frac{V_i}{I_b} = \frac{I_b . h_{ie} + (1+h_{fe})I_b R_E}{I_b}$$

$$= h_{ie} + (1+h_{fe})R_E$$

(d) To find input resistance $R_i = V_i/I_i$

$$R_i = \frac{V_i}{I_i} = \frac{V_i}{I_b} \cdot \frac{I_b}{I_i} = \frac{I_b . h_{ie} + (1+h_{fe})I_b R_E}{I_b} \cdot \frac{R_B}{R_B + h_{ie} + (1+h_{fe})R_E}$$

$$= \frac{\left[h_{ie} + (1+h_{fe})R_E\right].R_B}{R_B + h_{ie} + (1+h_{fe})R_E} \qquad = R_B \,||\left[h_{ie} + (1+h_{fe})R_E\right]$$

(e) To find output resistance R_0

$$R_0 = \frac{h_{ie}}{1+h_{fe}} \,||\, R_E = \frac{1}{g_m} ||\, R_E$$

(f) To find voltage gain $A_v = V_0 / V_i$

$$A_v = \frac{\text{Output Voltage } (V_0)}{\text{Input Voltage } (V_i)} \qquad = \frac{I_b(1+h_{fe}).R_E}{I_b.\left[h_{ie} + (1+h_{fe})R_E\right]}$$

$$= \frac{(1+h_{fe})R_E}{h_{ie} + (1+h_{fe})R_E}$$

Note : Since $(1 + h_{fe}) R_E >> h_{ie}$ and $h_{fe} >> 1$, we get $AV \cong 1$. Hence $V_0 = Vi$, the output voltage follows the input voltage. Hence the name voltage follower or buffer.

(g) To find current gain $A_I = I_0 / I_i$

$$A_i = \frac{\text{output current}}{\text{input current}} = \frac{I_0}{I_i} = \frac{I_0}{I_b} \cdot \frac{I_b}{I_i}$$

$$= \frac{(1+h_{fe})I_b}{I_b} \cdot \frac{R_B}{R_B + h_{ie} + (1+h_{fe})R_E} = \frac{(1+h_{fe}).R_B}{R_B + h_{ie} + (1+h_{fe})R_E}$$

Q.3(b) Draw and explain energy band diagram of MOS capacitor in accumulation, depletion and inversion region. [10]

(A) Case 1 : Accumulation

If a negative gate voltage V_G is applied to the gate electrode, the holes in the p-type substrate attracted to the semiconductor oxide interface.
This is called accumulation on the surface.
The oxide electric field is directed towards the gate electrode.
Electrons are pushed deeper into the substrate.

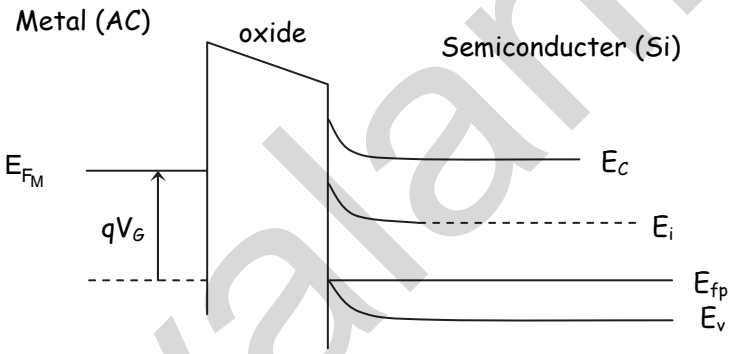
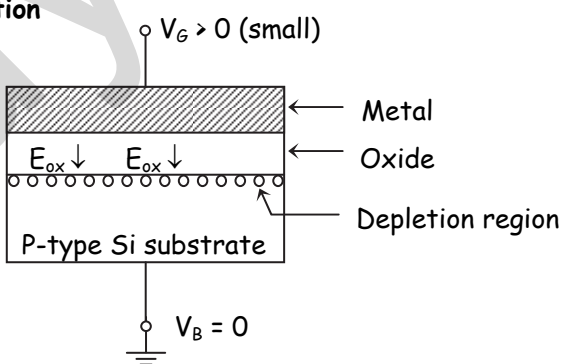


Fig. (a)

Case 2 : Depletion



A small positive gate bias V_G is applied to the gate electrode, since the substrate bias is zero. The oxide electric field will be directed towards the substrate.

Holes will be repelled back into the substrate. Thus a depletion region is created near the surface. In this condition, near the semiconductor oxide interface is nearly devoid of all mobile carriers.

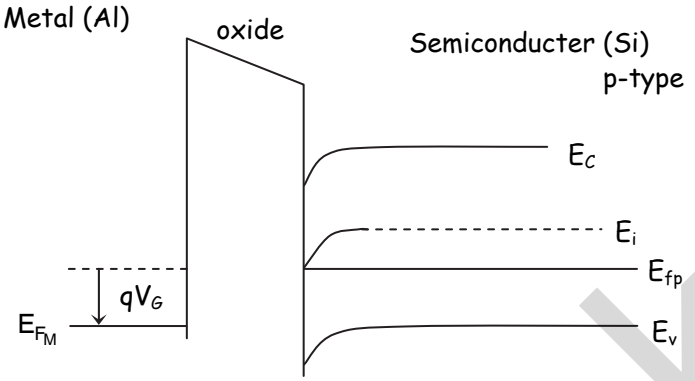
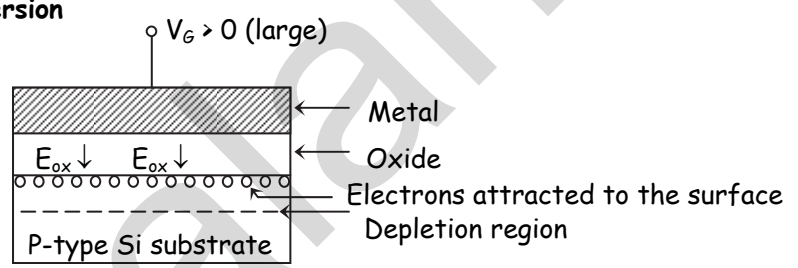


Fig. (b) : Energy band diagram of the MOS structure operating in depletion mode, under small gate bias.

Case 3 : Inversion



Due to increase in V_G, positive gate potential attracts additional minority carriers (electrons) from the substrate to the surface.

The n-type region created near the surface by the positive gate bias is called the inversion layer and this condition is called surface inversion.

This thin inversion layer on the surface with a large mobile electrons concentration can be utilised for conducting current between two terminals of the MOS transistor.

As a practical definition, the surface is said to be inverted when the density of mobile electron on the surface becomes equal to the density of holes in the bulk (p-type) substrate.

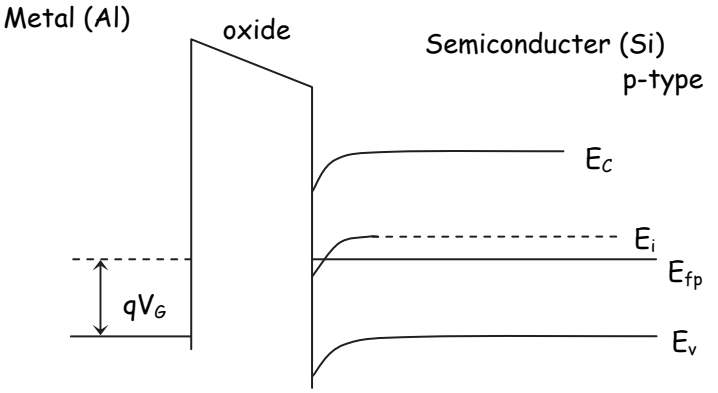
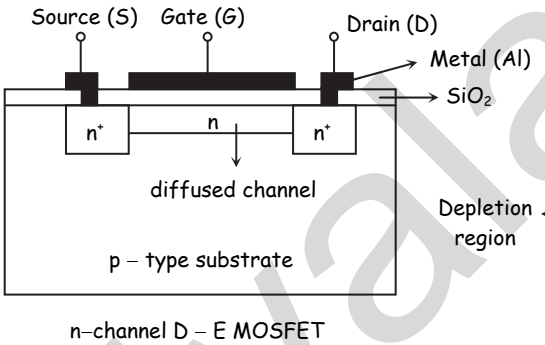


Fig. (c) : energy band diagram of the MOS structure in surface inversion, under larger gate bias voltage.

Q.4(a) Explain the basic operation and characteristics of n-channel depletion type MOSFET. [10]

(A)



n–channel D – E MOSFET

Fig. (a)

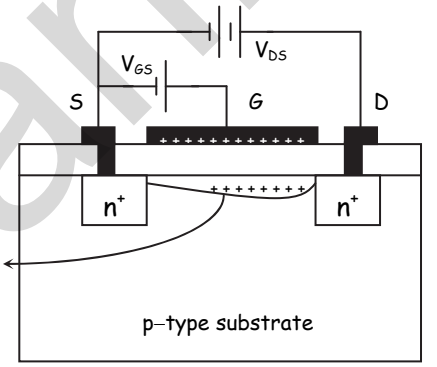


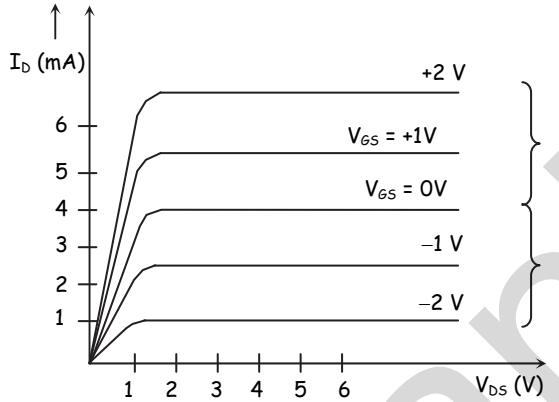
Fig. (b)

Fig. (a) shows the construction features of depletion enhancement MOSFET. The construction is the same as that for the enhancement mode MOSFET, except that a lightly doped n–channel has been introduced between the two heavily doped source and drain blocks.

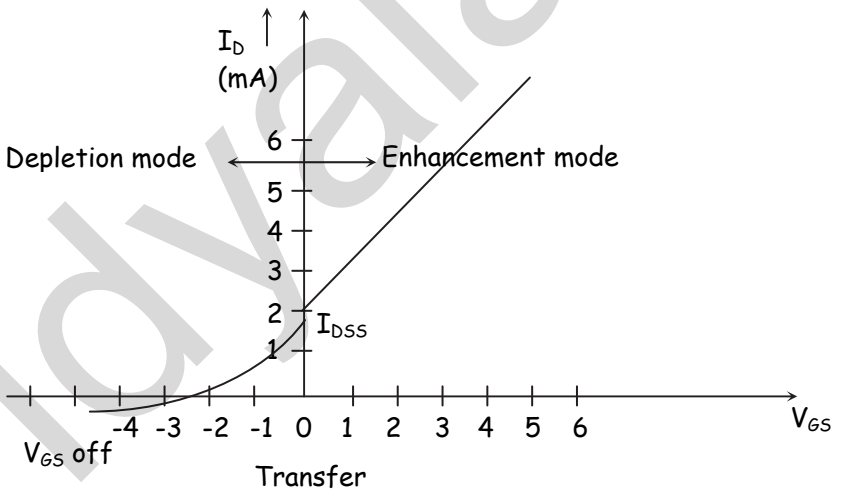
V–I characteristics of n – channel D – MOSFET

When the drain is made positive with respect to the source, appreciable drain current I_{DSS} flows, even with zero gate to source voltage (V_{GS} = 0), because electrons can flow from source to drain through n–type channel existing between them. If the gate is made negative with respect to the source, some of the negative charge carriers are repelled from the gate and driven out of the n-type channel, and cause the channel resistance to increase. Drain current drops as V_{GS} is made more negative. This effect is similar to that in the n–channel JFET. Since the action of negative voltage

on gate is to deplete the channel of free n–type charge carriers (which are majority charge carriers), the device operating with negative V_{GS} is referred to as depletion mode MOSFET, note [Fig. (b)], because of the voltage drop due to the drain current, the channel region nearest the drain is more depleted than is the region near the source. This phenomenon is similar to that of Pinch–off occurring in a JFET at the drain end of the channel, drain characteristic of depletion mode MOSFET and the JFET are quite similar.



Drain characteristic



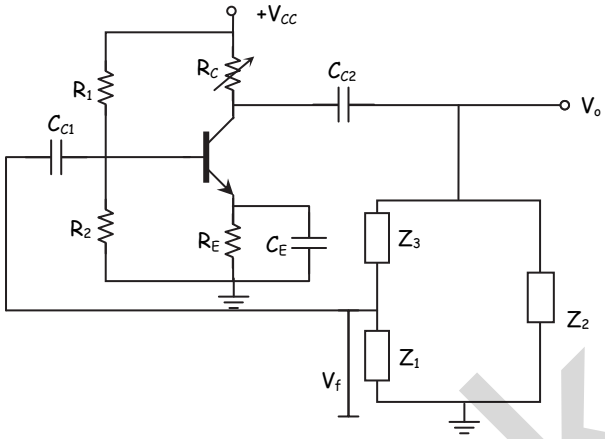
Transfer

Q.4(b) Draw a neat circuit diagram of Colpitts oscillator and derive an expression for its output frequency. [10]

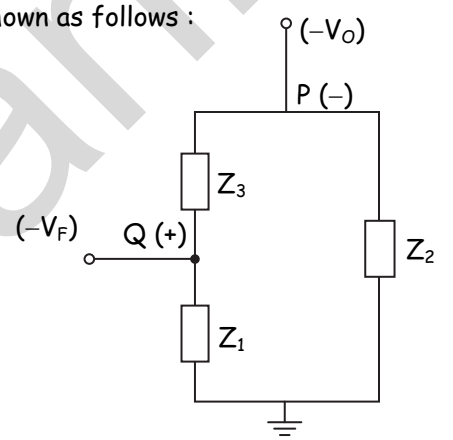
(A) Shift of 180° is due to centre tapped indicator or capacitor

Let $Z_1 = jX_1$, $Z_2 = jX_2$, $Z_3 = jX_3$ be the components of feedback network.

∴ Block diagram of LC oscillators can be shown :



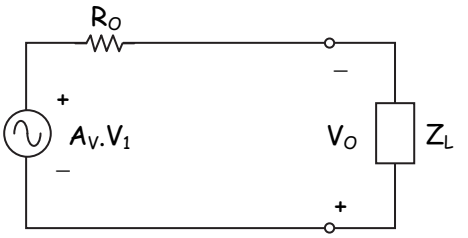
Under no feed back condition, Z_1 and Z_3 are in series and series combination in parallel with Z_2 therefore the load to the amplifier is $Z_2 = (Z_1 + Z_3) \parallel Z_2$
The modified feed back network can be shown as follows :



1) $V_P = \frac{Z_1}{Z_1 + Z_3}(-V_O)$

$\therefore \beta = \frac{V_F}{V_O} = -\frac{Z_1}{Z_1 + Z_3}$ ... (1)

2) The output of amplifier with the load can be shown as follows.



$V_O = -\frac{Z_L}{Z_L + R_O}(A_V.V_i)$

$\frac{V_O}{V_i} = AV_L = -\frac{A_V Z_L}{Z_L + R_O}$ ... (2)

3) $AV_L.\beta = \left(-\frac{A_V Z_L}{Z_L + R_O}\right)\left(-\frac{Z_1}{Z_1 + Z_3}\right)$

$= \left\{\frac{A_V\left[\frac{(Z_1 + Z_3)Z_2}{Z_1 + Z_2 + Z_3}\right]}{\left[\frac{(Z_1 + Z_3)Z_2}{Z_1 + Z_2 + Z_3}\right] + R_O}\right\}\left(\frac{Z_1}{Z_1 + Z_3}\right)$

$$A V_L.\beta = \frac{A_V.Z_1.Z_2}{Z_2(Z_1+Z_3)+R_O(Z_1+Z_2+Z_3)} \quad \ldots (3)$$

4) $Z_1 = jX_1, \quad Z_2 = jX_2, \quad Z_3 = jX_3$

$$\therefore \quad A V_L.\beta = \frac{-A_V X_1 X_2}{-X_2(X_1+X_3)+jR_O(X_1+X_2+X_3)} \quad \ldots (4)$$

5) To obtain the oscillators we must have $A\beta = 1 + jO$
Therefore image part of equation (4) should be zero.

$R_O (X_1 + X_2 + X_3) = 0$

$\therefore$ R_O is not zero.

$\therefore$ $X_1 + X_2 + X_3 = 0 \quad \leftarrow$ Condition 3

6) When imaginary part is zero, the real part is given by

$$A V_L.\beta = \frac{-A_V.X_1 X_2}{-X_2(X_1+X_3)} = \frac{A_V.X_1}{X_1+X_3} = \frac{A_V.X_1}{-X_2} \quad \left\{ \begin{matrix} X_1+X_2+X_3=0 \\ X_1+X_3=-X_2 \end{matrix} \right\}$$

$$= \frac{(-A_V)X_1}{X_2}$$

$$\therefore \quad A V_L.\beta = \frac{|A_V|X_1}{X_2} \quad \ldots (5)$$

For stability $AV_L.\beta > 1$

$$\therefore \quad \frac{|A_V|X_1}{X_2} \geq 1$$

$$\therefore \quad |A_V| \geq \frac{X_2}{X_1}$$

i.e. As the lefft side is magnitude, right side should be positive i.e. sign of X_1 and X_2 must be same i.e. both should be either inducctors or capacitor.
When X_1 and X_2 are capacitors, X_3 is Inductor, it is Colpitt's oscillator.

7) To obtain frequency of Oscillations

$$X_1 + X_2 + X_3 = 0$$

$$\frac{-1}{WC_1} - \frac{1}{WC_2} + WL = 0$$

$$\therefore \quad \frac{1}{W}\left(\frac{1}{C_1}+\frac{1}{C_2}\right) = WL$$

$$\frac{1}{W}\left(\frac{C_1+C_2}{C_1.C_2}\right) = WL$$

$$C_{eq} = \frac{C_1 C_2}{C_1+C_2}$$

$$\therefore \quad W^2 = \frac{1}{LC_{eq}}$$

$$W = \frac{1}{\sqrt{LC_{eq}}}$$

$$\therefore \quad f_O = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

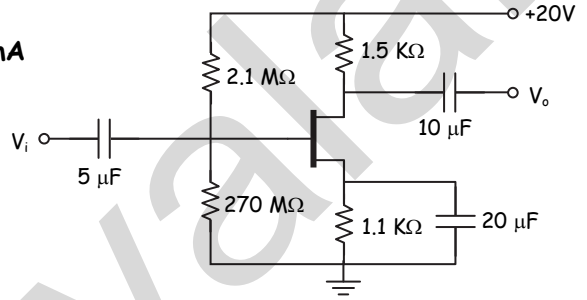
8) For stable oscillations, the required conditions is

$$|A_V| \geq \frac{X_2}{X_1} \geq \frac{\left(\frac{-1}{WC_2}\right)}{\left(\frac{-1}{WC_1}\right)}$$

$$\therefore \quad \frac{hf_e R_C}{h_{ie}} \geq \frac{C_2}{C_1}$$

Q.5(a) Determine I_{DQ}, V_{GSQ}, V_D and V_S for the network given below : [10]

I_{DS} = 10 mA
V_p = –4V



(A)

$v_g = \frac{270K}{270K + 2.1K} 20 = 2.278$ V

$R_g = 270K \,||\, 2.1K = 239.2$ KΩ

$V_{gs} = V_g - I_D R_S = 2.278 - 1.1 I_D$

$= -1.6$ N

$I_D = I_{DS}\left[1 - \frac{V_{gp}}{V_p}\right]^2 = 10\left[1 + \frac{2.278 - 1.1 I_D}{4}\right]^2$

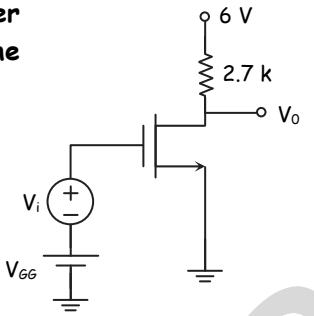
$= 3.54$ mA

$V_{DSQ} = V_{DD} - I_D [R_D + R_S] = 10.796$ V

$V_S = I_D R_S = 3.894$ V

$V_D = V_{DD} - I_D R_D = 14.69$ V

Q.5(b) Obtain g_m, r_o and Av for the amplifier circuit shown in figure. In which region the device is operating? Justify. **[10]**



V_{GSR} = 3V
V_{TN} = 1V
K_n = 0.8 mA/V²
λ = 0.018 V⁻¹

(A) (1) $I_{DQ} = kn (V_{GSQ} - V_{TN})^2$ = 3.2 mA

(2) $V_{DSQ} = V_{DD} - I_{DQ} RD$ = 2.6 ΔV

(3) $g_m = 2K (V_{GSQ} - V_{TN})$ = 3.2 mA/V

(4) $r_0 = (\lambda . I_{DQ})^{-1}$ = 17.36 kΩ

(5) $AV = V_0 / V_i$ = $-gm (r_0 \,||\, RD)$
= – 2.69
$|AV|$ = 2.69

Q.6 Write short notes on any FOUR : **[20]**

Q.6(a) Write short note on Mid-Point Biasing of JFET. **[5]**

(A) Consider a self bias JFET circuit as shown. The drain current is selected such that

$$I_{DQ} = \frac{I_{DSS}}{2}$$

For a JFET,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

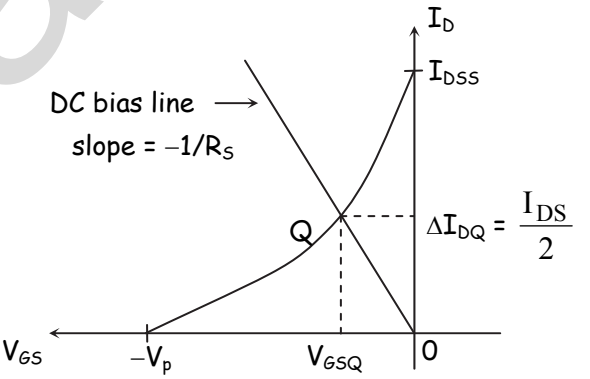
$$\therefore \quad \frac{I_{DSS}}{2} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\frac{1}{2} = \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\therefore \quad 0.707 = 1 - \frac{V_{GS}}{V_p}$$

$$\therefore \quad \frac{V_{GS}}{V_p} = 1 - 0.707 = 0.3$$

$$\therefore \quad V_{GS} = 0.3\, V_p$$



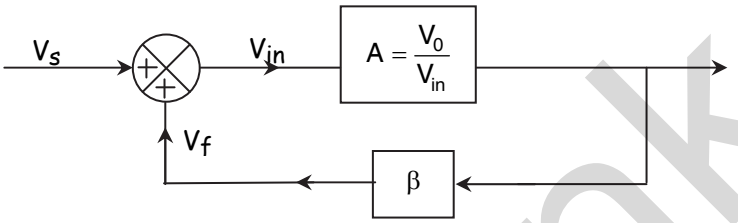
The significance of midpoint biasing technique is (refer class notes)

(a) It is the point on the transfer characteristics where we get maximum transconductance, and hence high gain. Such a JFET circuit can be used for amplifying weak signals.

(b) The point on the transfer characteristics where we get high g_m leads to a Q point which is highly unstable. Hence to get high gain and good stability we use mid point biasing.

Q.6(b) Write short note on Barkhusen criteria for sustained oscillations. [5]

(A)



$V_f = \beta V_0$

$V_f = A\,\beta V_{in}$

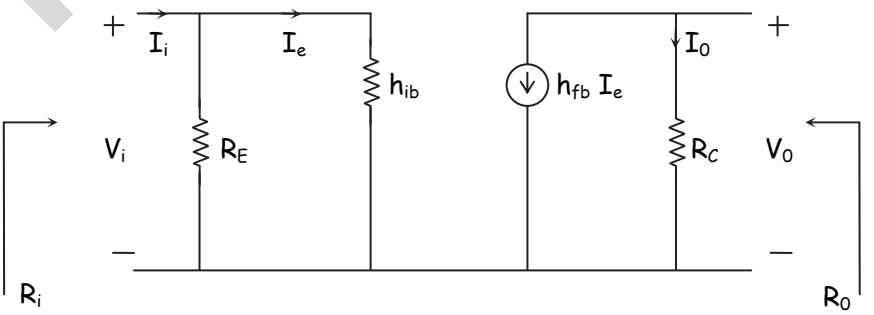
1) The frequency at which sinusoidal oscillator will operate is the frequency for which total phase shift introduced, as the signal proceeds from input terminal to the output of the amplifier and from output to feedback network and back to input terminal is precisely 360° or 0°. i.e., total phase shift around a closed loop should be 360° or 0° at oscillating frequency.

2) Oscillation will not be developed if at the oscillating frequency the product of magnitude of gain of amplifier i.e. A and a feedback factor of a feedback network i.e. β(+ve) is less than unity. Hence for sustained oscillation $A\beta = 1$.

Q.6(c) Write short note on Small signal equivalent circuit of CB amplifier [5]

(A) The Small signal equivalent circuit of CB amplifier is as shown.

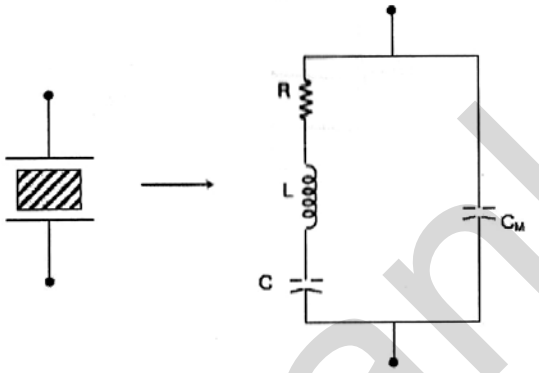
Replace transistor by its h parameter model



Q.6(d) Write short note on Crystal oscillator. [5]

(A) A crystal oscillator is basically a tuned circuit oscillator using a piezoelectric crystal as a resonant lank circuit. The crystal has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are widely used in communication transmitters and receivers.

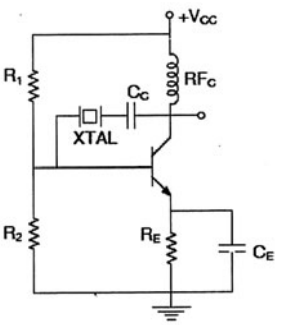
Electrical equivalent circuit of a crystal



Here, inductor L and capacitor c represents electrical equivalents of crystal mass and compliance. R is electrical equivalent of the crystal structure's internal fraction. C_M is the capacitance due to mechanical mounting of the crystal.

Crystal controlled oscillator

To operate a crystal in the series resonant made it may be connected as a series element in a feedback path. A typical transistor circuit is as shown in figure.



Resistor R_1, R_2 and R_E provide a voltage divider stabilized bias circuit. Capacitor C_E provides ac bypass of the emitter resistor and the RFC coil provides the dc bias while decoupling any ac signal on the power lines from affecting the output signal.

The voltage feedback from collector to base is maximum when the crystal impedance is minimum. The coupling capacitor C_C has negligible impedance at the circuit operating frequency but blocks any dc between collector and base. The circuit frequency stability is set by the crystal frequency stability which is good.

Q.6(e) Write short note on BJT as a switch. **[5]**

(A) BJT as a switch

Switching circuits are significantly different than linear circuits. They are also easier to understand. Before investigating more complex circuits, we will begin by introducing discrete solid-state switching circuits: those built around BJTs.

A switch consists of a BJT transistor that is alternately driven between the saturation and cutoff regions. A simple version of the switch is shown in figure 1. When the input equals $-V_{in}$, the base-emitter junction is reverse biased or off so no current flows in the collector. This is illustrated by the load line shown in the figure. When the BJT is in cutoff, the circuit (ideally) has the following values:

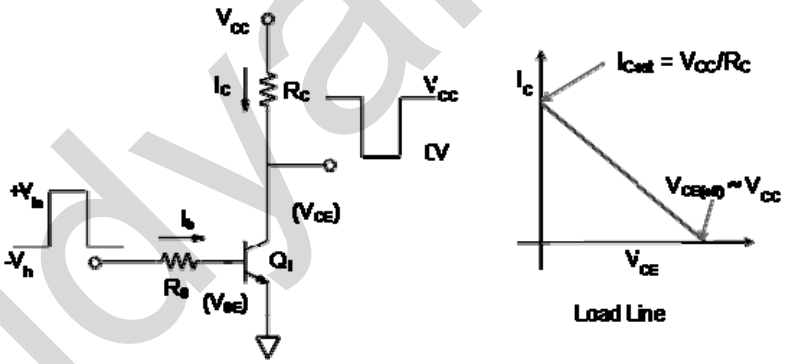
$V_{CE} = V_{CC}$ and $I_C = 0$ A

This state is similar to an open switch.

When the input equals $+V_{in}$, the transistor is driven into saturation and the following conditions occur:

$V_{CE=}$ 0V and $I_{Csat} = V_{CC}/R_C$

This state is similar to a closed switch connecting the bottom of R_C to ground.



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