S.E. Sem. III [ETRX]

Digital Circuits and Design

Time : 3 Hrs.] Prelim Question Paper **[Marks : 80**

N.B.: (1) Question No. **1** is **compulsory**.
(2) Solve any **Three** from remaining **Five** questions.
(3) Draw neat logic diagram and assume suitable data wherever necessary.

1. (a) Draw truth table and logic diagram of full adder. **[4]**
(b) Explain universal shift register. **[4]**
(c) Compare synchronous and asynchronous counters. **[4]**
(d) Explain Stuck at 0 and 1 faults. **[4]**
(e) What are the advantages and disadvantages of Quine McCluskey method **[4]**

2. (a) Explain IC 74163 with diagram. **[8]**
(b) Design Moore type sequence detector to detect a serial input sequence of 101. **[12]**

3. (a) Design MOD-5 synchronous counter using T flip-flop. **[10]**
(b) Explain Xilinx XC 9500 CPLD architecture. **[10]**

4. (a) Design a 2 bit comparator using gates. **[12]**
(b) Explain JTAG and BIST. **[8]**

5. (a) Design a sequence detector to detect the sequence of 101011. **[10]**
(b) Compare Moore and Mealy models. **[10]**

6. (a) Design a 4 bit, 4 state ring counter using IC 74194. **[10]**
(b) Write VHDL codes for the following : **[10]**
(i) SR flip flop (ii) 4 bit shift register

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