**Q.1 Solve following :** **[20]**

**Q.1(a) Explain characteristics of logic families.** **[5]**

**Ans.:** Characteristics of logic families are as follows :

1. Voltage and current parameters
2. Speed of operation
3. Power dissipation
4. Figure of merit
5. Fan-out
6. Noise immunity
7. Operating temperature range
8. Power supply requirements
9. Flexibilities available

**Speed of Operation :** The speed of a digital circuit is specified in terms of the propagation delay time. The delay times are measured between the 50 percent voltage levels of input and output waveforms. The propagation delay time of the logic gate is taken as the average of the two delay times.

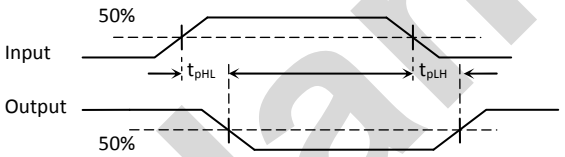



**Fig.:** Input and output voltage waveforms to define propagation delay times.

**Power Dissipation :** It is the amount of power dissipated in an IC. It is determined by the current, $I_{CC}$, that it draws from the $V_{CC}$ supply and is given by $V_{CC} \times I_{CC}$.

**Fan-Out :** This is the number of similar gates which can be driven by a gate. High fan-out is advantageous because it reduces the need for additional drivers to drive more gates.

**Q.1(b) State and Prove Demorgan Theorem.** **[5]**

**Ans.:** De-Morgan's Theorem :

This theorem states that the complement of a product is equal to addition of the complements.

Theorem 1 : $\overline{A.B} = \overline{A} + \overline{B}$ , NAND = Bubbled OR

| A | B | $\overline{A.B}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| | | ↑ |

| $\overline{A}$ | $\overline{B}$ | $\overline{A} + \overline{B}$ |
|---|---|---|
| 1 | 1 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |
| | | ↑ |

LHS = $\overline{A.B}$ = $\overline{A} + \overline{B}$ = RHS

Theorem 2 : $\overline{A+B} = \overline{A}.\overline{B}$ , NOR = Bubbled AND

| A | B | $\overline{A+B}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
| | | ↑ |

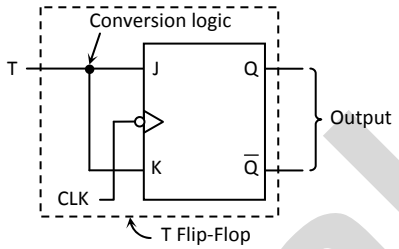
| $\overline{A}$ | $\overline{B}$ | $\overline{A}.\overline{B}$ |
|---|---|---|
| 1 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 0 | 0 | 0 |
| | | ↑ |

LHS = $\overline{A+B} = \overline{A}.\overline{B}$ = RHS

**Q.1(c) Convert JK flip flop to T flip flop.** **[5]**

**Ans.:**

| Q | $Q_{n+1}$ | J | K | T |
|---|---|---|---|---|
| 0 | 0 | 0 | X | 0 |
| 0 | 1 | 1 | X | 1 |
| 1 | 0 | X | 1 | 1 |
| 1 | 1 | X | 0 | 0 |




For J :

| $Q_n$ \ T | 0 | 1 |
|---|---|---|
| 0 | 0 | 1 |
| 1 | X | X |

J = T

For K :

| $Q_n$ \ T | 0 | 1 |
|---|---|---|
| 0 | X | X |
| 1 | 0 | 1 |

K = T

| $Q_n$ \ T | 0 | 1 |
|---|---|---|
| 0 | 0 | X |
| 1 | 1 | X |

J = T

| $Q_n$ \ T | 0 | 1 |
|---|---|---|
| 0 | X | 0 |
| 1 | X | 1 |

K = T

**Q.1(d) Convert the following numbers as mentioned against them:** **[5]**

**(I) $(101011)_2$ convert to decimal number.**

**(II) Convert $(129.625)_{10}$ Hexadecimal form.**

**(III) Write $(-20)_{10}$ in Two's complement form.**

**Ans.: (i) $(101011)_2$ convert to decimal number**

$$\begin{matrix} 1 & 0 & 1 & 0 & 1 & 1 \\ 2^5 & 2^4 & 2^3 & 2^2 & 2^1 & 2^0 \end{matrix}$$

$= 32 + 8 + 2 + 1 = 43$

$\therefore (101011)_2 = (43)_{10}$

**(ii) Convert $(129.625)_{10}$ Hexadecimal form :**

| | | | |
|---|---|---|---|
| 16 | 129 | 1 | ↑ $0.625 \times 16 = 10$ |
| 16 | 8 | 8 | |
| | 0 | | |

$(129.625)_{10} = (81.A)_{16}$

**(iii) Write $(-20)_{10}$ in Two's complement for m**

| | | |
|---|---|---|
| 2 | 20 | 0 |
| 2 | 10 | 0 |
| 2 | 5 | 1 |
| 2 | 2 | 0 |
| 2 | 1 | 1 |
| | 0 | |

$\therefore$ $(20)_{10} = 10100 = (00010)_{2's}$

$00010100 \rightarrow (11101100)_{2's}$

$\therefore$ $(-20) = 11101100$

**Q.2(a) Minimize the following expression using Quine McCluskey technique : [10]**

**$F(A,B,C,D) = \Sigma(0,1,2,3,5,7,9,11)$**

**Ans.:** Step 1 :

| Minterm | Binary representation | | | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |
| 11 | 1 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 |

Step 2 : Grouping as per no. of 1's

| Minterm | Binary representation | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | ✓ | 0,1 | 0 | 0 | 0 | – | ✓ |
| 1 | 0 | 0 | 0 | 1 | ✓ | 0,2 | 0 | 0 | – | 0 | ✓ |
| 2 | 0 | 0 | 1 | 0 | ✓ | 3,1 | 0 | 0 | – | 1 | ✓ |
| 3 | 0 | 0 | 1 | 1 | ✓ | 1,5 | 0 | – | 0 | 1 | ✓ |
| 5 | 0 | 1 | 0 | 1 | ✓ | 1,9 | – | 0 | 0 | 1 | ✓ |
| 9 | 1 | 0 | 0 | 1 | ✓ | 2,3 | 0 | 0 | 1 | – | |
| 11 | 1 | 0 | 1 | 1 | ✓ | 3,11 | – | 0 | 1 | 1 | ✓ |
| 7 | 0 | 1 | 1 | 1 | | 9,11 | 1 | – | 0 | 1 | ✓ |
| | | | | | | 3,7 | 0 | – | 1 | 1 | |
| | | | | | | 5,7 | 0 | 1 | – | 1 | |

| Minterm | Binary representation | | | | | Minterm | Binary representation | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0,1,2,3 | 0 | 0 | – | – | | 0,1,2,3 | 0 | 0 | – | – |
| 0,2,3,1 | 0 | 0 | – | – | | 1,3,9,11 | – | 0 | – | 1 |
| 1,3,9,11 | – | 0 | – | 1 | | 1,3,5,7 | 0 | – | – | 1 |
| 1,9,3,11 | – | 0 | – | 1 | | | | | | |
| 1,3,5,7 | 0 | – | – | 1 | | | | | | |

| Prime implicants | Binary Representation | | | |
|---|---|---|---|---|
| | A | B | C | D |
| 0,1,2,3 | 0 | 0 | – | – |
| 1,3,9,11 | – | 0 | – | 1 |
| 1,3,5,7 | 0 | – | – | 1 |

| Minterm Group | $m_0$ | $m_1$ | $m_2$ | $m_3$ | $m_5$ | $m_9$ | $m_{11}$ | $m_7$ |
|---|---|---|---|---|---|---|---|---|
| 0,1,2,3 | • | • | • | • | | | | |
| 1,3,9,11 | | • | | | • | • | • | |
| 1,3,5,7 | • | | | • | • | | | • |

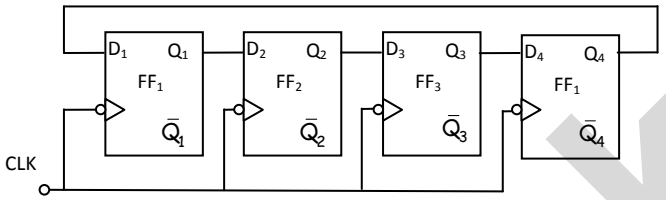
(1,5,9,11) (0,1,2,3) (1,3,5,7)

Y = – 0 – 1 + 0 0 – – + 0 – – 1

Y = $\bar{A}D$ + $\bar{B}D$ + $A\bar{B}$

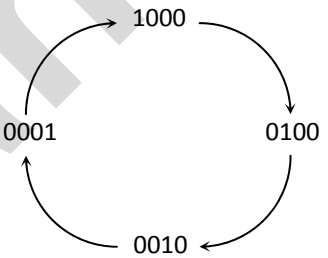
**Q.2(b) Draw four bit Ring counter and explain its operation. [10]**

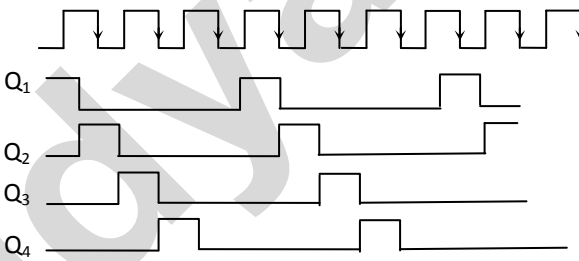
**Ans.:**




| Sequence Table | | | | After clock pulse |
|---|---|---|---|---|
| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | |
| 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 1 | 3 |
| 1 | 0 | 0 | 0 | 4 |
| 0 | 1 | 0 | 0 | 5 |
| 0 | 0 | 1 | 0 | 6 |
| 0 | 0 | 0 | 1 | 7 |

State Diagram

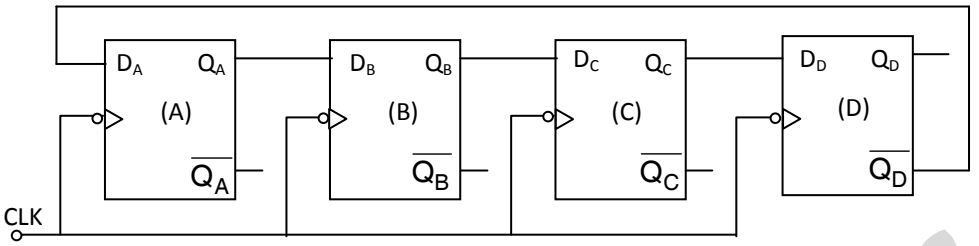



The FFS are arranged such that Q output of each stage is connected to the D input of next stage, but the Q output of the last flip flop is connected back to the D input of first FF such that array of FF is arranged in a ring. Initially the first FF is preset to a 1, so the initial state is 1000. After each clock pulse the contents of the shift register are shifted to the right by one bit & $Q_4$ is shifted to $Q_1$. The Sequence repeats after 4 clock pulses.

**Q.3(a) Explain the Johnson's Counter. Design for initial state 0110. From initial state explain and draw all possible states. [10]**

**Ans.:** In a Johnson counter, the Q output of each stage of flip-flop is connected to the D input of the next stage.

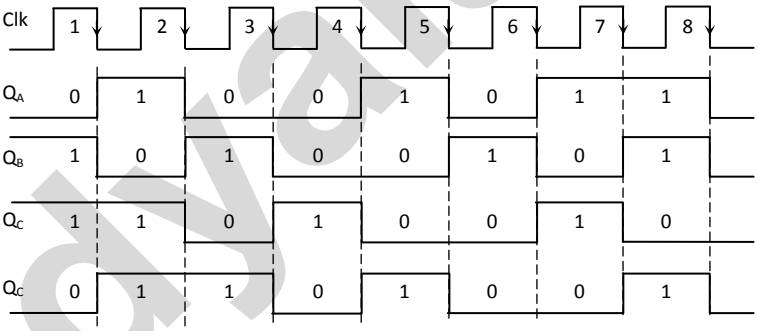



Four bit Johnson Counter

| Decimal Number | Clock Pulse | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
|---|---|---|---|---|---|
| 6 | 0 | 0 | 1 | 1 | 0 |
| 11 | 1 | 1 | 0 | 1 | 1 |
| 5 | 2 | 0 | 1 | 0 | 1 |
| 2 | 3 | 0 | 0 | 1 | 0 |
| 9 | 4 | 1 | 0 | 0 | 1 |
| 4 | 5 | 0 | 1 | 0 | 0 |
| 10 | 6 | 1 | 0 | 1 | 0 |
| 13 | 7 | 1 | 1 | 0 | 1 |

Initially, the register is kept at state 0110 (initial state). So all the outputs $Q_A$, $Q_B$, $Q_C$, $Q_D$ consist of specified output at initial state. Therefore, complement output of last stage, $Q_D$ is one as the output of $Q_D$ at initial state is zero. This is connected back to first stage ($D_A$). Hence, $D_A$ is one.

**Timing Diagram :**




An n-stage Johnson counter will produced a modulus of $2 \times n$, where n is the number of stages (i.e. flip-flops) in the counter.

**Q.3(b) Implement the following function using only one 4:1 multiplexer and gates : [10]**

**$Y = F(A,B,C,D) = \sum m\ (2, 3, 5, 7, 10, 11, 12, 13)$**

**Ans.:**

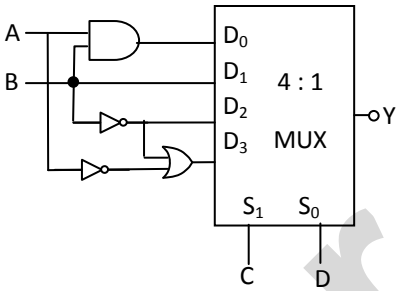
| | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
|---|---|---|---|---|
| $\bar{A}\bar{B}$ | 0 | 1 | (2) | (3) |
| $\bar{A}B$ | 4 | (5) | 6 | (7) |
| $A\bar{B}$ | 8 | 9 | (10) | (11) |
| $AB$ | (12) | (13) | 14 | 15 |

$D_0 = AB$

$D_1 = \bar{A}B + A\bar{B} = B(A + \bar{A}) = B$

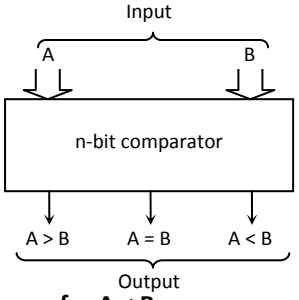
$D_2 = \bar{A}\bar{B} + A\bar{B} = \bar{B}(\bar{A} + A) = B$

$D_3 = \bar{A}\bar{B} + \bar{A}B + AB = \bar{A} + A\bar{B} = \bar{A} + \bar{B}$




**Q.4(a) Design a 2 bit comparator and implement using logic gates.** **[10]**

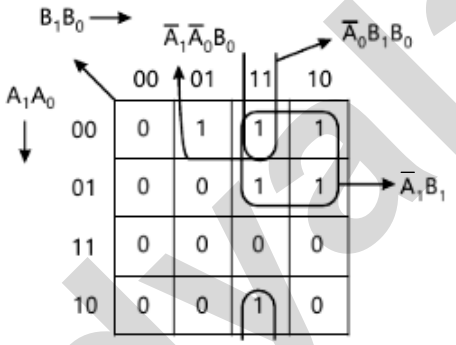
**Ans.:**




Truth table:

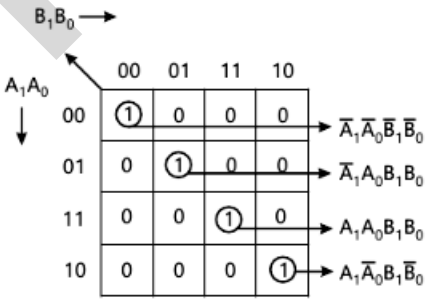
| Input | | | | Output | | |
|---|---|---|---|---|---|---|
| $A_1$ | $A_0$ | $B_1$ | $B_0$ | A < B | A = B | A > B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

**K-map for A < B :**



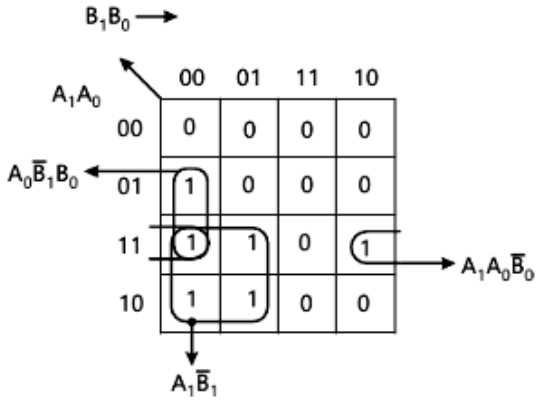

$\therefore (A < B) = \bar{A}_1 B_1 + \bar{A}_0 B_1 B_0 + \bar{A}_1 \bar{A}_0 B_0$

**K-map for A = B :**



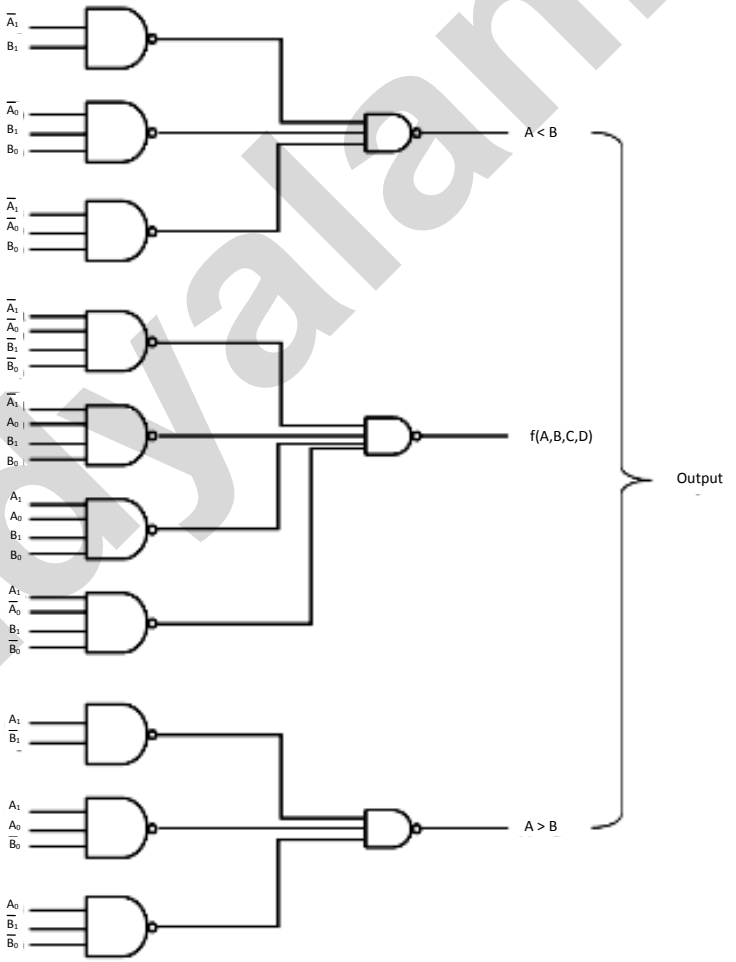

$\therefore (A = B) = \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 B_1 B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0$

**K-map for A > B**



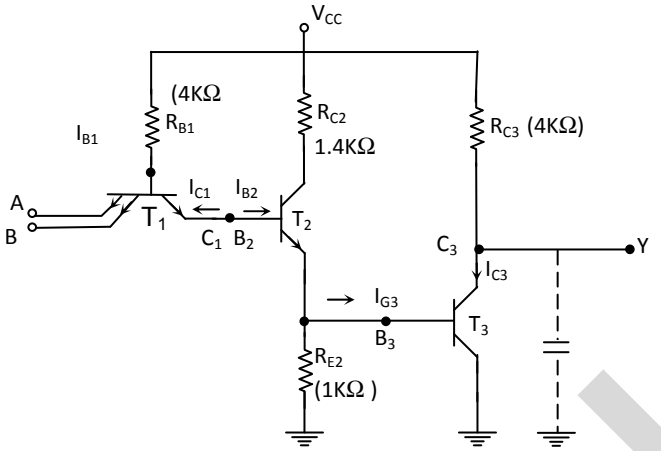

$\therefore (A > B) = A_1\overline{B}_1 + A_1A_0\overline{B}_0 + A_0\overline{B}_1\overline{B}_0$

**Implementation :**



**Q.4(b) Draw circuit diagram of 2 input TTL NAND gate and explain its operation. [10]**

**Ans.:**




Assume load gates are not present & the voltages for logic 0 & 1 are $V_{CE}$ = 0.2V & $V_{CC}$ = 5V

**Condition 1 (Atleast one input is LOW) :**

The B–E junction of $T_1$ corresponding to the input in the LOW state is forward biased making voltage at $B_1$ $VB_1$ = 0.2 + 0.7 = 0.9V.

For B–C junction of $T_1$ to be forward biased & for $T_2$ & $T_3$ to be conducting $V_{01}$ required to be at least 0.6 + 0.5 + 0.5 = 1.6 V. Hence $T_2$ & $T_3$ are OFF.

$\therefore$ Y = $V_{CC}$

**Condition 2 (All inputs are HIGH) :**

B.E junction of $T_1$ is reverse biased. If we assume $T_2$ & $T_3$ are ON then $V_{B2}$ = $V_{C1}$ = 0.8 + 0.8 = 1.6V. Since $B_1$ is connected to $V_{CC}$ (5V) through $R_{B1}$, C–B junction of $T_1$ is forward biased. The transistor $T_1$ is operating in active inverse mode, making $I_{C1}$ flow in the reverse direction. This current flows in the base of $T_2$ & $T_3$ into saturation.

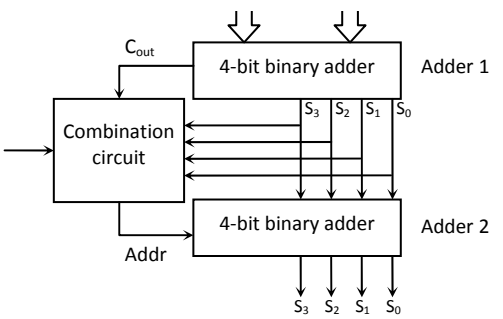
$\therefore$ Y = 0.2 V

**Condition 3 :**

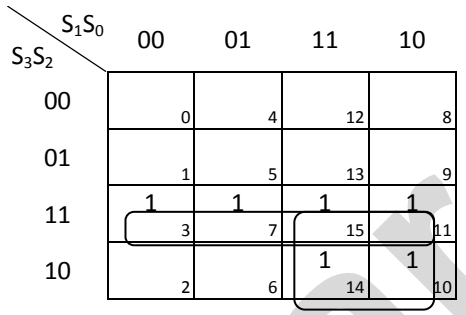
Let the circuit be operating under condition 2, when one of the inputs suddenly goes to V(0). The corresponding E–B junction of $T_1$ starts conducting & $V_{B1}$ drops to 0.9V – $T_2$ & $T_3$ will be turned off when the stored charge is removed since $V_{C1}$ = $V_{B2}$ = 1.6V, C-B junction of $T_1$ is back biased, making $T_1$ operate in the normal active mode. This large current of $T_1$ is in a direction which helps in the removal of stored base charge in $T_2$ & $T_3$ & improves speed of the circuit.

**Q.5(a) Design BCD Adder using the integrated circuit 4 bit binary adders. [10]**

**Ans.:**




(correct BCD answer)




| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |

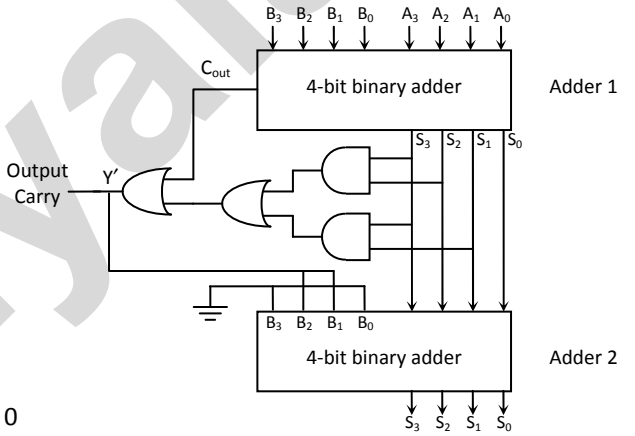
Sum is valid BCD number
$\therefore$ Y = 0

| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Y |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Sum is invalid BCD number
$\therefore$ Y = 1

$Y = S_3S_2 + S_3S_1$

Equation for combinational circuit




1) Sum $\leq$ 9, Carry = 0

If sum is less than or equal to 9 and carry is zero then there is no need to add 0110 to get BCD number as it is already valid BCD number.

2) Sum > 9, Carry = 0

If sum is greater than 9 than it is invalid BCD number hence 0110 (6) is added to sum to get valid BCD number.

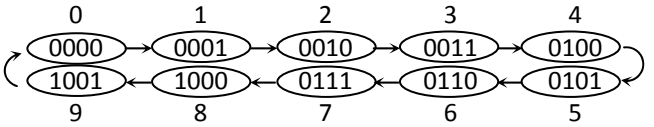
3) Sum $\leq$ 9, Carry = 1

If sum is less than 9 but carry is 1 that means the BCD number is more than 9 hence 0110 (6) is added to it.

**Q.5(b) Design lockout free mod 10 up synchronous counter using JKMS flip flops. [10]**

**Ans.:** Step 1: No. of FFS : $N \leq 2^n$ $10 \leq 2^n$ $\therefore$ n = 4

Step 2: State diagram




Excitation table for J–K flip–flop

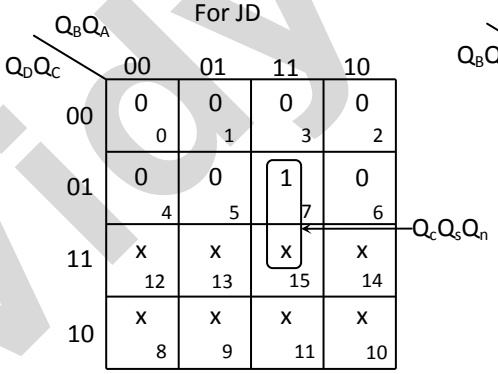
| Present State | Next state | J | K |
|---|---|---|---|
| Q | $Q_{n+1}$ | | |
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

Circuit excitation table :

| Present State | | | | Next State | | | | Flip–Flop inputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ | $Q_{D+1}$ | $Q_{C+1}$ | $Q_{B+1}$ | $Q_{A+1}$ | $J_D$ | $K_D$ | $J_C$ | $K_C$ | $J_B$ | $K_B$ | $J_A$ | $K_A$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | X | 0 | X | 0 | X | 1 | X |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | X | 0 | X | 1 | X | X | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | X | 0 | X | X | 0 | 1 | X |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | X | 1 | X | X | 1 | X | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | 0 | 0 | X | 1 | X |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | 0 | 1 | X | X | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | 0 | X | 0 | 1 | X |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | X | X | 1 | X | 1 | X | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | X | 0 | 0 | X | 0 | X | 1 | X |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | 1 | 0 | X | 0 | X | X | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | 1 | 0 | X | X | 1 | 0 | X |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | X | 1 | 0 | X | X | 1 | X | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | X | 1 | X | 1 | 0 | X | 0 | X |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | X | 1 | X | 1 | 0 | X | X | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | X | 1 | X | 1 | X | 1 | 0 | X |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | X | 1 | X | 1 | X | 1 | X | 1 |

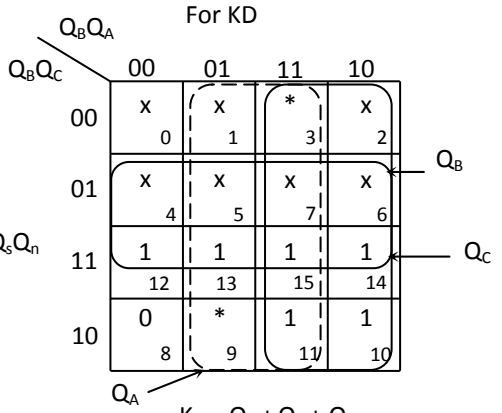
K-maps :

For JD



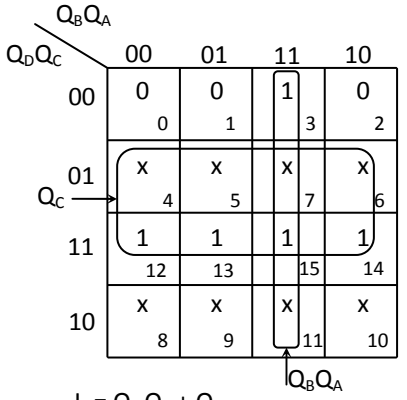

$J_D = Q_CQ_BQ_A$

For KD



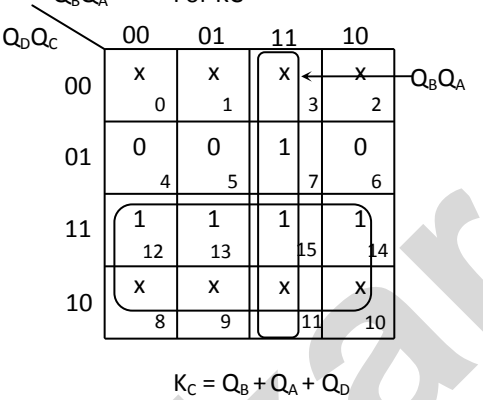

$K_D = Q_A + Q_B + Q_C$

For JC



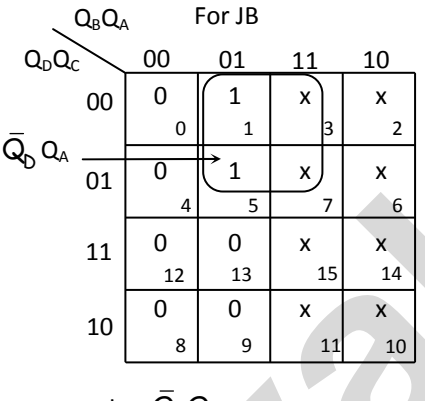

$J_C = Q_B Q_A + Q_C$

For KC



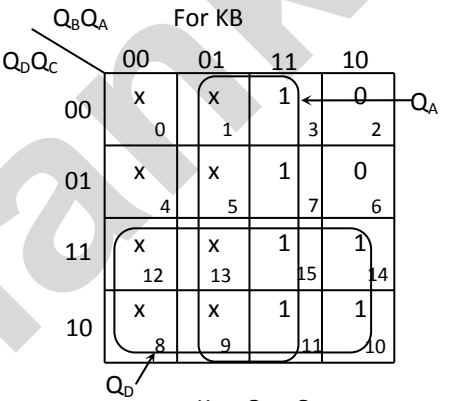

$K_C = Q_B + Q_A + Q_D$

For JB



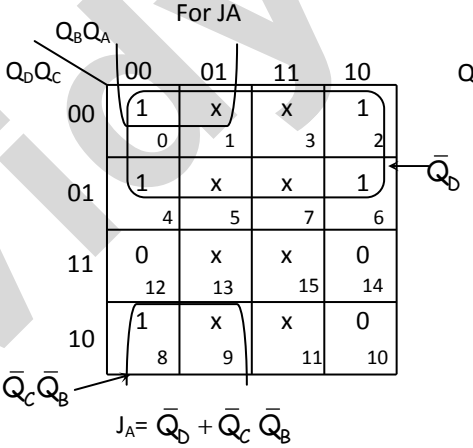

$J_B = \bar{Q}_D Q_A$

For KB



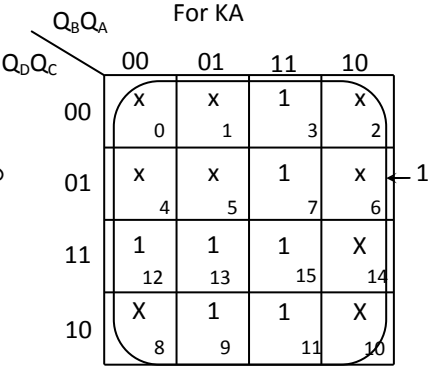

$\therefore K_B = Q_D + Q_A$

For JA



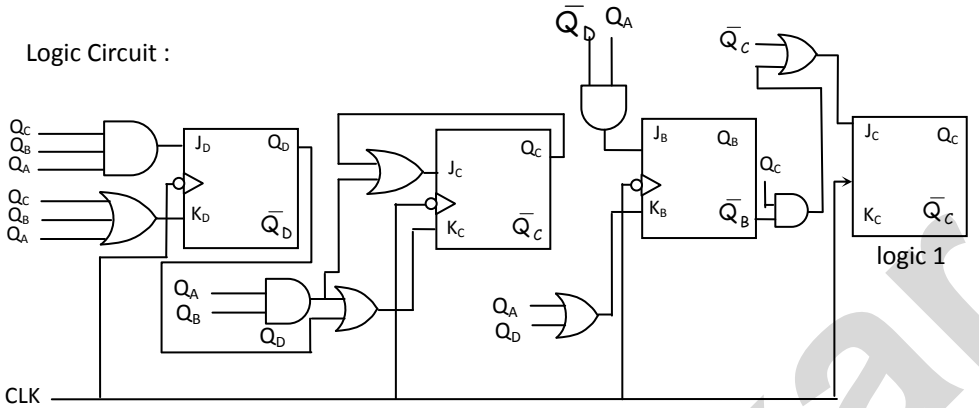

$J_A = \bar{Q}_D + \bar{Q}_C \bar{Q}_B$

For KA




$K_A = 1$

Logic Circuit :




**Q.6 Write short notes on following : [20]**

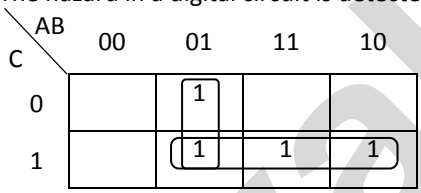
**Q.6(a) Write short note on Hazards. [5]**

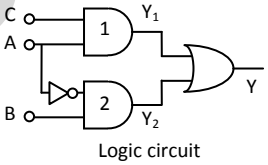
**Ans.: Hazards :**

The electronic components used have associated propagation delays because of which the changes in response of a circuit do not occur instantaneously with the changes in the input. This may result in an unwanted phenomena known as Hazard.

**Detection of Hazard :**

The hazard in a digital circuit is detected b using K-map of the circuit :




Logic circuit

$\Delta t_1$ and $\Delta t_2$ are the propagation delays of paths through AND gate 1 and 2 respectively.

**Types of Hazards :**

In case of hazard occurring in SOP form of realization the output goes to 0 momentarily when it should have remained 1, and in POS form its vice versa. The first type refers to static-1 hazard and second type refers to static-0 hazard. A third type of hazard, known as dynamic hazard, causes the output to change number of times when it should change from 1 to 0 or from 0 to 1.

**Q.6(b) Write short note on Hamming Code. [5]**

**Ans.: Hamming Code :**

Hamming code is an error-correcting code. It is constructed by adding a number of parity bits to each group of n-bit information or message in such a way so as to be able to locate the bit position in which error occurs. Let us assume K parity bits $P_1$, $P_2$, ..... $P_k$ are added to the n-bit message to form an (n + k) bit code.

$2^k \geq n + k + 1$

The location of each of the n + k bits within a code word is assigned a decimal number, starting from 1 to the MSB and n + k to the LSB. K parity checks are performed on selected bits of each code word. Each parity check includes one of the parity bits. The result of

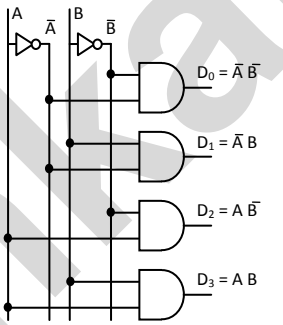
each parity check is recorded as 1 if error has been detected and as 0 if no error has been detected. The parity bits $P_1$, $P_2$, … $P_k$ are placed in locations 1, 2, 4, …$2^{k-1}$.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $P_1$ | $P_2$ | $D_0$ | $P_3$ | $D_1$ | $D_2$ | $D_3$ | $P_4$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_8$ | $D_9$ | $D_{10}$ | $P_5$ |

**Q.6(c) Write short note on Encoder and Decoder. [5]**

**Ans.:** **Encoder :** An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has $2^n$ input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value. In encoders it is assumed that only one input has a value of 1 at any given time, otherwise the circuit is meaningless.

**Decoder :** A decoder is a combinational circuit that converts binary information from n input lines to a maximum of $2^n$ unique output lines.




Here, 2 inputs are decoded into four output each output representating one of the minterms of the 2 inputs variables.

**Q.6(d) Compare TTL and CMOS logic families. [5]**

**Ans.:**

| Parameter | CMOS | | TTL | | | |
|---|---|---|---|---|---|---|
| | Silicon gate CMOS | Metal gate CMOS | 74 | 7425 | 74AS | 74A25 |
| $V_{1H(min)}$ | 3.5 | 3.5 | 2.0 | 2.0 | 2.0 | 2.0 |
| $V_{1L(max)}$ | 1.0 | 1.5 | 0.8 | 0.8 | 0.8 | 0.8 |
| $V_{0H(min)}$ | 4.9 | 4.95 | 2.4 | 2.7 | 2.7 | 2.7 |
| $V_{0L(max)}$ | 0.1 | 0.05 | 0.4 | 0.5 | 0.5 | 0.4 |
| $V_{NH}$ | 1.4 | 1.45 | 0.4 | 0.5 | 0.7 | 0.7 |
| $V_{NL}$ | 0.9 | 1.45 | 0.4 | 0.3 | 0.3 | 0.4 |
| Propagation delay | 8 | 105 | 10 | 10 | 1.5 | 4 |
| Power per gate (mV) | 0.17 | 0.1 | 10 | 2 | 8.5 | 1 |
| Speed power | 1.4 pJ | 10.5 pJ | 100 pJ | 20 pJ | 12.8 pJ | 4 pJ |
| Product or figure of merit in connection | Input cannot be left open. It has to be connected to O or to $V_{DD}$ or to another input | | Input can be left open. It is treated as logic high input. | | | |
| Power dissipation | Very less | | More than CMOS | | | |
| Fan-out | Fan-out is more than TTL(50) | | Fan-out for TTL is 10 | | | |
| Noise | More susceptible to noise | | Less susceptible to noise | | | |

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