S.E. Sem. III [ETRX]

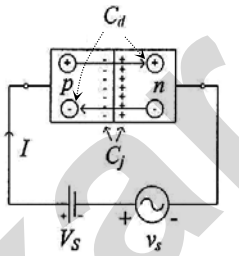
Electronic Circuits and Design – I

Time : 3 Hrs.] Prelim Paper Solution **[Marks : 80**

Q.1(a) What happens when diode is operated at high frequency? [5]

Ans.: Diode High Frequency Model :

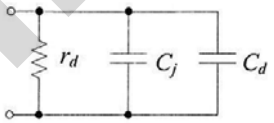
This purely resistive AC model for the diode works well when the frequency of the AC signals is sufficiently low.



At high frequencies, we need to include the effects that arise due to these time varying signals and the charge separation that exists in the depletion region and in the bulk *p* and *n* regions of the diode under forward bias conditions.

Within the device and the depletion region there exists an electric field. For AC signals, this electric field is varying with time.

As you've learned in electromagnetics, a time varying electric field is a displacement current. The effects of a displacement current are modeled by equivalent circuit capacitances :



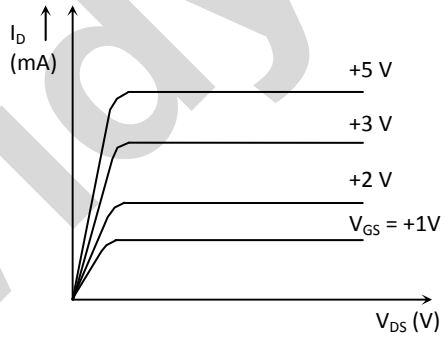
We won't do anything with this effect now. This is presented primarily as an FYI.

Q.1(b) Explain why CC configuration is referred as Voltage follower. [5]

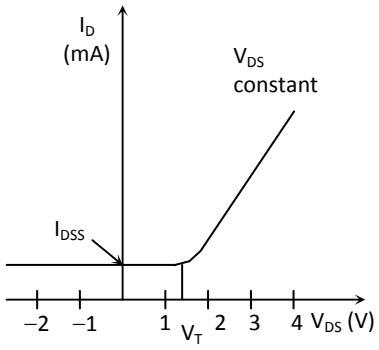
Ans.: As CC amplifier provides Av = 1 = $\frac{Vo}{Vi}$. Implies that Vo = Vi, i.e. output follows input, hence the name voltage follower

Q.1(c) Draw transfer and drain characteristics of E–MOSFET. [5]

Ans.: The transfer and drain characteristics of E–MOSFET is as shown



Drain characteristics



Transfer characteristics

Q.1(d) Explain construction of Schottky diode and draw its characteristics. [5]

Ans.: It is mainly used as a rectifier at signal frequency exceeding 300 MHz due to it's quick response time and lower noise Figure. It has more uniform junction region and is more rugged than PIN diode.

Construction :

It is a metal–semiconductor junction diode with no depletion layer. It uses a metal (like gold, silver, platinum, tungsten etc.) on one side of junction and usually an N type doped silicon semi–conductor on the other side. The diode construct & its symbol are shown in above Figure.

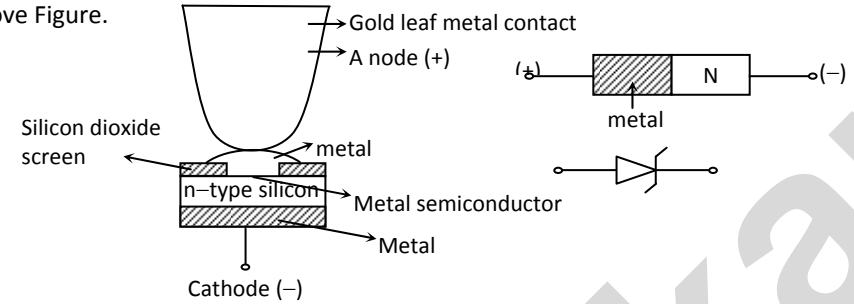


Fig. 1: Schottky Barrier diode (a) basic structure (b) symbol

Applications :

1) Because of these quality schottky diode can easily rectify signals of frequencies exceeding 300 MH_3, it can produce an almost perfect half wave rectified output.
2) It is commonly used in switching power supplied that operates at frequencies of 20 GHz.
3) Due to low noise Figure it is extremely important in communication receivers and radar units etc.

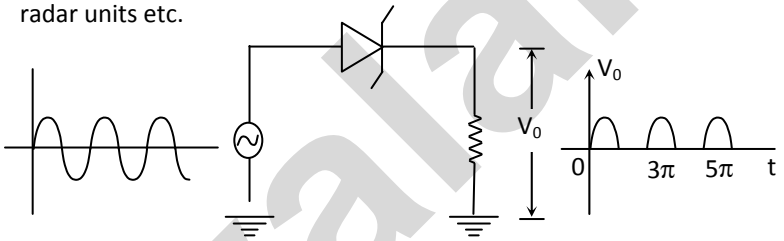
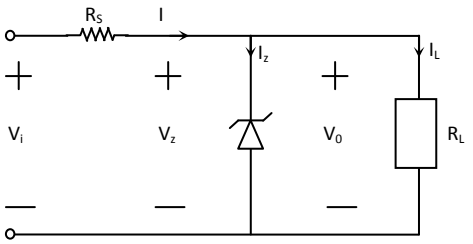


Fig. 2 : Application of Schottky Barrier diode as rectifier.

Q.1(e) What is the Voltage Regulator explain simple zener shunt voltage Regulator. [5]

Ans.: A regulator is an electronic circuit that provides constant and stabilized output independent of variation of applied input voltage.

The Zener Shunt Regulator is as shown.

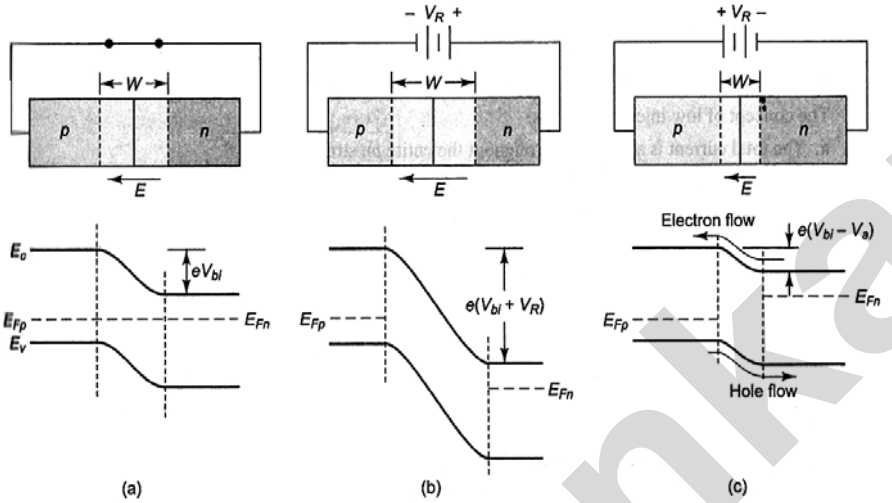


The circuit diagram of zener shunt regulator is as shown. The zener is connected in shunt with the load, and zener is kept reverse biased. The unregulated input V_i must be greater than V_0 , atleast by 5 to 10 V. The resistor R_S will ensure a minimum current through zener when $V_i = V_{i\ min}$, keeping the zener in ON state. Also it limits the maximum value of zener current when $V_i = V_{i\ max}$.

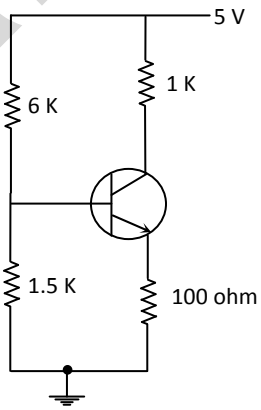
In the ON state, zener maintains a constant voltage across its terminals. Therefore $V_0 = V_z$. Since V_z is a stable zener reference source, the output voltage is stable and hence the load gets a constant voltage.

Q.2(a) **Draw Energy band diagram of pin junction diode under :** **[10]**
(i) Zero Bias, (ii) Forward bias and (iii) Reverse Bias

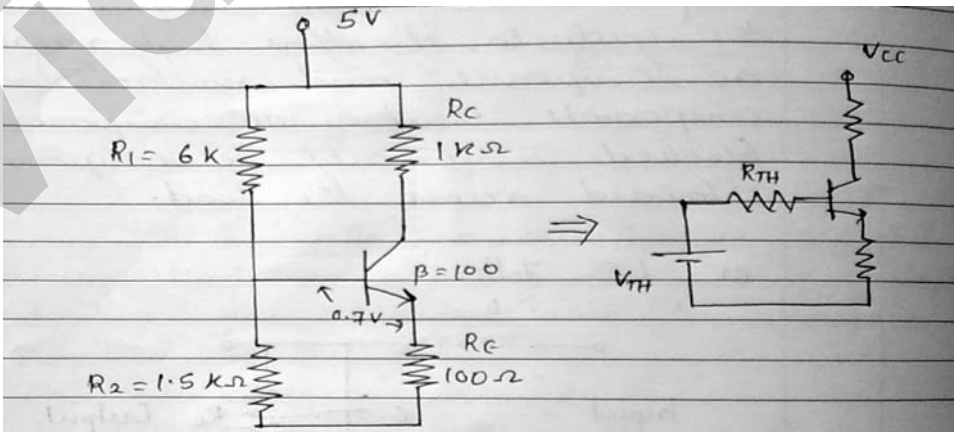
Ans.: (a) zero bias, (b) reverse bias, and (c) forward bias



Q.2(b) For the given circuit find Steady State DC Parameters I_{cq} and V_{ceq} **[10]**
Given β = 100 and V_{BE} = 0.7 V,
also state in which region the circuit is working.



Ans.:



$$R_{TH} = R_B = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{(6K)(1.5K)}{(6K + 1.5K)} = 1.2K\Omega$$

$$V_{TH} = V_B = V_{CC} \cdot \left(\frac{R_2}{R_1 + R_2}\right) = 5\left(\frac{1.5K}{7.5K}\right) = 1V$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta) R_E} = \frac{1 - 0.7}{1.2K + (101)(100)}$$

$$= 2.654 \times 10^{-5} A$$

$$I_{C_Q} = \beta I_B$$

$$= 100 (2.65 \times 10^{-5})$$

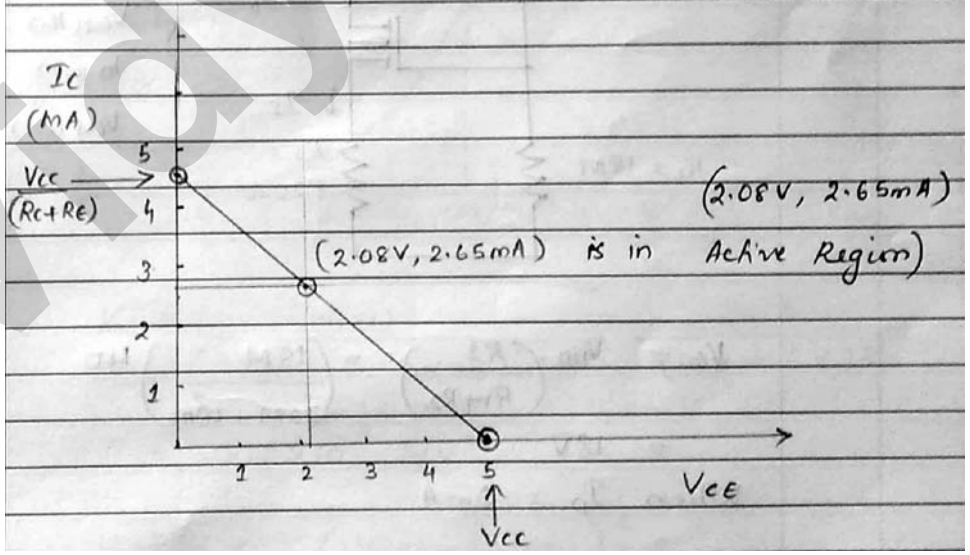
$$= \underline{2.654 \text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C R_C - I_E R_E$$

$$= V_{CC} - I_C (R_C + R_E)$$

$$= 5 - 2.654m (1K + 100\Omega)$$

$$= \underline{2.0806 V}$$



To draw dc load line

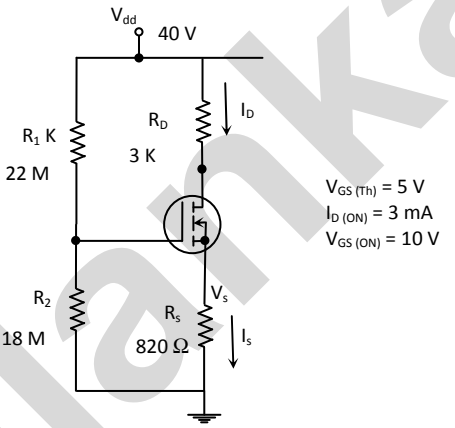
$V_{CE} = V_{CC} - I_C (R_C + R_E)$

(a) When $I_C = 0$; $V_{CE} = V_{CC} = 5V$

(b) When $V_{CE} = 0$ $I_C = V_{CC}/(R_C + R_E) = 4.54 mA$

The transistor for the given circuit is working in active region.

Q.3(a) **For the given MOSFET amplifier, Determine I_{Dq}, V_{GSq} and V_{DS}.** **[10]**



Ans.:

$V_G = V_{DD} \cdot \left(\frac{R_2}{R_1 + R_2}\right) = \left(\frac{18M}{22M + 18M}\right) 40$

$= 18 V$

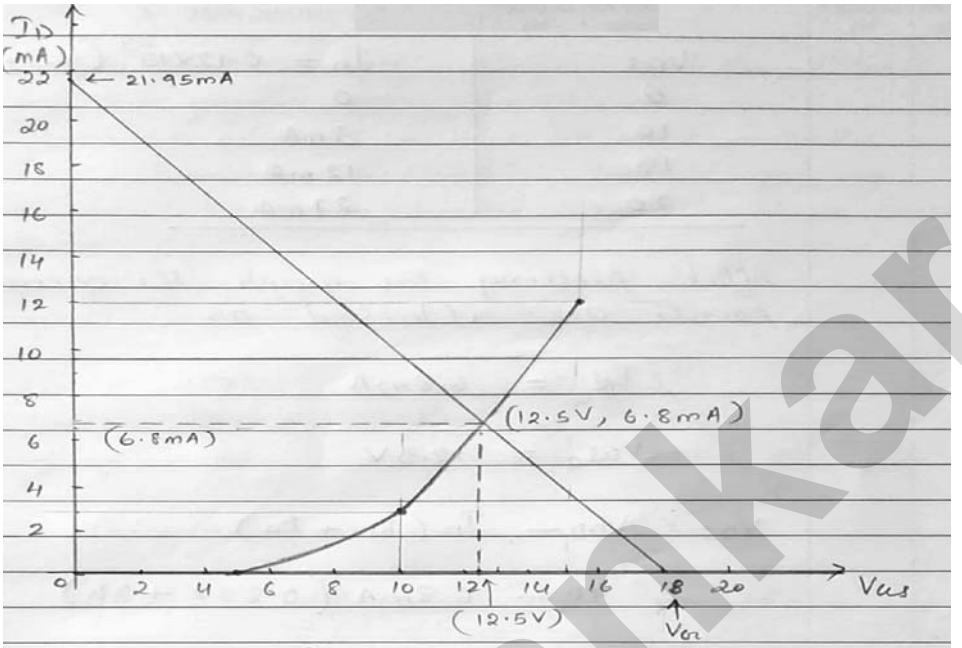
When $I_D = 0 mA$

$V_{GS} = 18V - (0mA)(0.82K) = 18V$

When $V_{GS} = 0V$

$0 = 18V - I_D (0.82K)$

$I_D = \frac{18V}{0.82K} = 21.95 mA$



$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(TH)})^2} = \frac{3mA}{(10V - 5V)^2}$$

$$= 0.12 \times 10^{-3} \ A/V^2$$

$$\therefore I_D = K(V_{GS} - V_{GS(TH)})^2$$

$$= 0.12 \times 10^{-3} (V_{GS} - 5)^2$$

V_{GS}	$I_D = 0.12 \times 10^{-3} (V_{GS} - 5)^2$
5	0
10	3 mA
15	12 mA
20	27 mA

After plotting the graph the operating points are obtained as

$$I_{D_Q} = 6.8mA$$

$$V_{GS_Q} = 12.5V$$

$V_{DS} = V_{DD} - I_D (R_S + R_D)$

$= 40 - 6.8mA\ (0.82K + 3K)$

$= 14.024$

Q.3(b) Explain working principle, characteristics and applications of Tunnel diode. [10]

Ans.: Tunnel diode is a specially made p-n junction device which exhibits negative resistance over part of the forward bias characteristic. It has extremely heavy doping on both sides of the junction and an abrupt transition from the p-side to the n-side. The tunneling effect is a majority carrier effect and is consequently very fast. The tunnel diode is useful for oscillation or amplification purposes. Because of the thin junction and short transit time, it is also useful for microwave applications in fast switching circuits.

Volt-amp Characteristics of a Tunnel Diode

The volt-ampere characteristics of a tunnel diode are shown in Figure below.

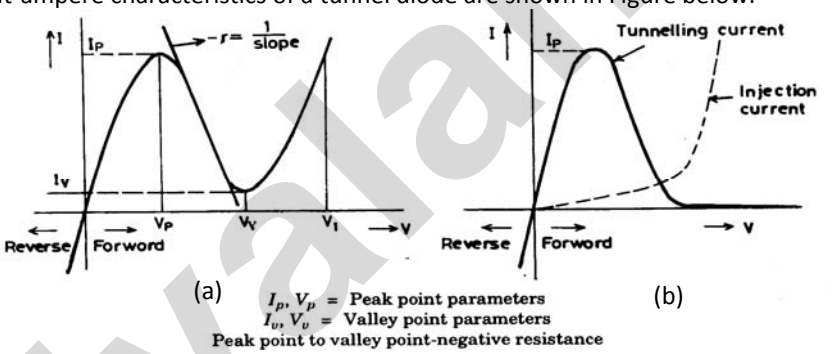


Fig. 1 : (a) Sum of tunneling and injection, (b) V-I characteristic of tunnel diode.

The tunnel effect controls the current at very low values of forward bias where the normal or the injection current is very small as shown in Figure above. The mechanism of tunneling is purely a quantum mechanical phenomenon. An electron on one side of the barrier will have a certain probability of leaking through the barrier if barrier is very thin. If both p and n type materials of a junction are heavily doped, the depletion region becomes very narrow; as narrow as of the order of 100 A.

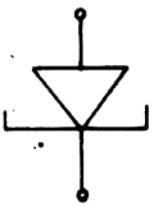
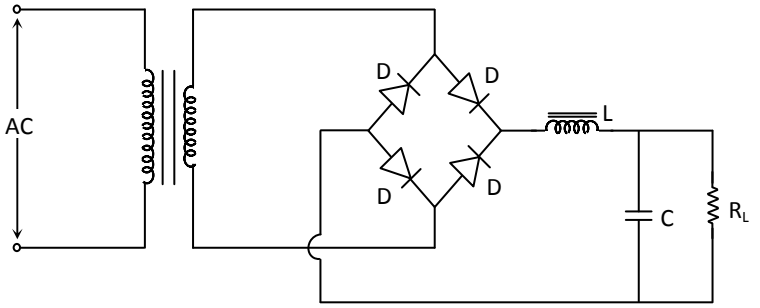


Fig. 2: Symbol for tunnel diode

Q.4(a) Derive expression for ripple factor for L–section filter. [10]

Ans.: **L. C. Filter :**

In case of L filter the ripple factor γ is directly proportional to the R_L, whereas in c Filter, the ripple factor γ is inversely proportional to R_L, it means in both the circuit γ depends upon the R_L, to overcome the above problem, we use LC Filter, which is combination of L & C filter, and in LC Filter the ripple factor γ is independent of load resistance R_L.



As shown in the figure, the rectifier output is given to the inductor. The inductor provides more opposition to the AC component and less opposition to the DC component. This results that, most of the AC component appears across the inductor and whole of the DC component passes to the load. If at all any part part of AC component manages to reach the load, then it is removed by the capacitor C.

Derivation for Ripple Factor :

Assumption Mode :

i) While obtaining the expression for the ripple factor, we will consider only the second harmonics component and neglect all other higher order harmonics.

ii) Inductive Reactance X_L > Capacitive Reactance X_C.

The Full wave Rectifier output is pulsating in nature, hence its Fourier Series is given as :

$$= \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2wt - \frac{4V_m}{15}\cos 4wt$$

Neglecting higher order harmonics.

$$= \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2wt$$

In the above equation $\frac{2V_m}{\pi}$ represents the d.c. component available at the output of Rectifier and $\frac{4V_m}{3\pi}\cos 2wt$ represents the AC component available at the Rectifier output.

The peak value of the AC current is given as :

$$I_{(peak)} = \frac{\frac{4V_m}{3\pi}\cos 2wt}{X_L}$$

Assuming cos 2 wt = 1,

$$I_{(peak)} = \frac{4V_m}{3\pi X_L}$$

$$\therefore \quad I_{RMS} = \frac{I_{(peak)}}{\sqrt{2}} = \frac{4V_m}{3\pi\sqrt{2}X_L} \qquad = \frac{2}{3\sqrt{2}X_L} \cdot \frac{2V_m}{\pi} \qquad \text{But} \quad \frac{2V_m}{\pi} = V_{dc}$$

$$\therefore \quad I_{RMS} = \frac{2}{3\sqrt{2}X_L} \cdot V_{dc}$$

$$\therefore \quad I_{RMS} = \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{X_L}$$

Now the RMS voltage developed across the load is given as :

$$V_{RMS} = I_{RMS} \cdot X_L$$

$$\therefore \quad V_{RMS} = \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{X_L} \cdot X_C$$

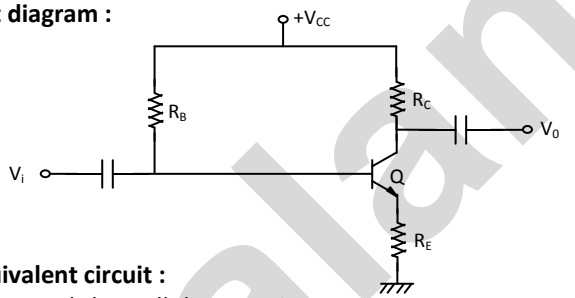
$$\therefore \quad \frac{V_{RMS}}{V_{dc}} = \frac{\sqrt{2}}{3} \cdot \frac{X_C}{X_L}$$

$$\therefore \quad \gamma = \frac{\sqrt{2}}{3} \cdot \frac{X_C}{X_L} \qquad \text{where } X_C = \frac{1}{2wC} \ \& \ X_L = 2wL$$

Q.4(b) Derive expression for Input resistance, Voltage gain, current gain and output resistance for CE amplifier with R_E unbypassed. [10]

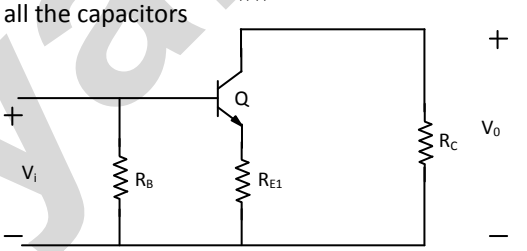
Ans.: Common Emitter BJT Amplifier with R_E unbypassed

(a) Circuit diagram :

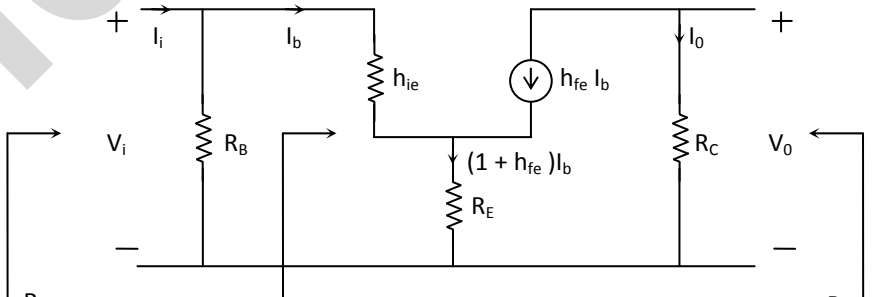


(b) ac Equivalent circuit :

Short V_{CC} and short all the capacitors



(c) Replace transistor by its h parameter model :



$$\frac{V_i}{I_b} = \frac{I_b \cdot h_{ie} + (1 + h_{fe}) I_b R_E}{I_b}$$

$$= h_{ie} + (1 + h_{fe}) R_E$$

(d) To find input resistance $R_i = V_i/I_i$:

$$R_i = \frac{V_i}{I_i} = \frac{V_i}{I_b} \cdot \frac{I_b}{I_i} = \frac{I_b . h_{ie} + (1 + h_{fe}) I_b R_E}{I_b} \cdot \frac{R_B}{R_B + h_{ie} + (1 + h_{fe}) R_E}$$

$$= \frac{\left[h_{ie} + (1 + h_{fe}) R_E\right] . R_B}{R_B + h_{ie} + (1 + h_{fe}) R_E} \qquad = R_B \,||\left[h_{ie} + (1 + h_{fe}) R_E\right]$$

(e) To find output resistance R_0 :

$R_0 = R_C$

(f) To find voltage gain $A_v = V_0 / V_i$:

$$A_v = \frac{\text{Output Voltage } (V_0)}{\text{Input Voltage } (V_i)} \qquad = \frac{I_0 . R_C}{I_b . \left[h_{ie} + (1 + h_{fe}) R_E\right]}$$

$$= -\frac{h_{fe} I_b R_C}{I_b \left[h_{ie} + (1 + h_{fe}) R_E\right]} \qquad = -\frac{h_{fe} R_C}{h_{ie} + (1 + h_{fe}) R_E}$$

The –ve sign indicates that input and output voltages are 180° out of phase.

(g) To find current gain $A_I = I_0 / I_i$

$$A_i = \frac{\text{output current}}{\text{input current}} \qquad = \frac{I_0}{I_i} \qquad = \frac{I_0}{I_b} \cdot \frac{I_b}{I_i} \qquad = -\frac{h_{fe} I_b}{I_b} \cdot \frac{R_B}{R_B + h_{ie} + (1 + h_{fe}) R_E}$$

Q.5(a) Design Single Stage CE amplifier for the given specifications [10]
$A_v \geq 100$, S = 10, V_o = 3 V, f_L = 20 Hz and Ri > 3KΩ, also calculate Av, Ri and Ro for the designed circuit.

Ans.: Step 1: Selection of bias
We select voltage divider bias with R_E partially by-passed.

Step 2: Selection of transistor
We select BC 147.3 having following parameters.

P_{Dmax} = 250 mW	I_{cmax} = 0.1 A	V_{CEO} 45 V
h_{fe} = 330	h_{ie} = 4.5 KΩ	$V_{CE\ sat}$ = 0.25 V

Step 3: Design of R_C
Let R_2 = 10 KΩ and A_V = 22

$$|A_V| = \frac{h_{fe} . R_C'}{h_{ie} + (1 + h_{fe}) R_{E1}}$$

Let R_{E1} = 100 Ω; ¼ W

R_C' = 1.253 KΩ $\qquad \therefore \frac{R_E . R_C}{R_E + R_C}$ = 1.253 k

$\therefore$ R_C = 1.432 KΩ
$R_{C\ sat}$ = 1.5 KΩ; ¼ W

Step 4: To determine DC Q point,
$V_{CEQ} = 1.5\ [V_{CE\ sat} + V_{op}] \quad = 1.5\ [0.25 + 3] \quad = 4.875$ V

Let $V_{CEQ} = \frac{V_{cc}}{2}$ (mid point biasing)

$\therefore \quad V_{cc} = 9.75$ V

Let $V_{cc} = 10$ V

Let $V_{RE} = 10\% V_{cc} = 2$V

$\therefore \quad I_C = \frac{V_{CC} - V_{CE} - V_{RE}}{R_C}$

$\therefore \quad I_C = 2.75$ mA

Step 5: Design of R_E

$R_E = \frac{V_{RE}}{I_C} = 363\ \Omega$ $\qquad R_E = R_{E1} + R_{E2}$

$\therefore \quad R_{E2} = 263\ \Omega$

$R_{E2\ sat} = 240\ \Omega$; ¼ W

Step 6: Design of R_1 & R_2

Given $S = 10 = 1 + \frac{R_3}{R_E}$ $(R_E = R_{E1} + R_{E2}) = 340\ \Omega$

$R_3 = \frac{R_1.R_2}{R_1 + R_2} = 9.R_E = 3060$

$V_B = V_{BC} + V_{RE} = 0.7 + 1 = 1.7$V

also, $V_B = \frac{R_2}{R_1 + R_2}.V_{CC}$

$\therefore \quad \frac{R_2}{R_1 + R_2} = \frac{V_3}{V_{CC}} = 0.17$

$R_1 = 18$ KΩ $\qquad R_2 = 3.68$ KΩ

$R_{1\ sat} = 17$ KΩ; ¼ W $\qquad R_{2\ sat} = 3.6$ KΩ; ¼ W

To maintain $R_1 = 312\ \Omega$, let $R_2 = 4.3$ KΩ; ¼ W

Step 7: Design of capacitor

(a) $R_i = R_1 \,||\, R_2 \,||\, (h_{ie} + (1 + h_{fe})\, R_{E1}) = 3.14$ KΩ

$f_{LCC1} = \frac{1}{2\pi R_i C_{C1}}$, given $f = 20$ H_E, $C_{C1} = 2.5$ µf

$C_{C1\ sat} = 10$ µf; 5 V

(b) $R_0 = R_C + R_2 = 11.5$ KΩ

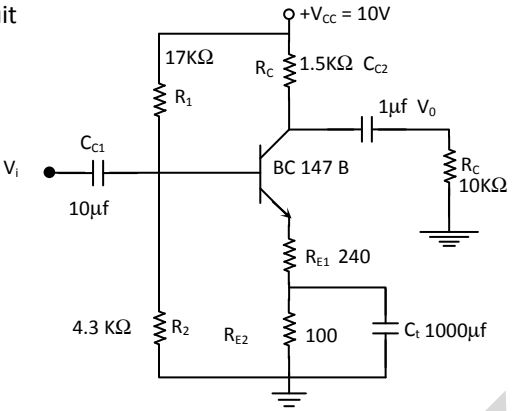
$f_{LCC2} = \frac{1}{2\pi R_0 C_{C2}}$ $\qquad C_{C2} = 0.69$ µf

$C_{C2\ sat} = 1$µf; 15 V

(c) $f_{LCC} = \frac{10}{2\pi R_E.C_E}$ $\qquad C_E = 796$ µf

$C_E = 1000$ µf; 5 V

Step 8: Designed Circuit



Step 9: Calculation for derived circuit

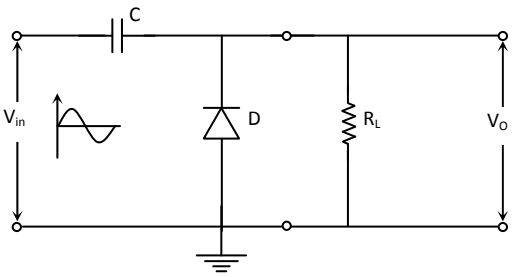
1. $R_0 = R_C' = 1.2\ K\Omega$
2. $R_i = R_C \,||\, R_2 \,||\, [h_{ie} + (1 + h_{fe})\, R_{C1}] \quad = 3.144\ K\Omega$
3. $|A_0| = \dfrac{h_{fe}.R_C'}{h_{ie} + (1 + h_{fe})\, R_{E1}} \quad = 10.53$

Q.5(b) What is Clamping circuit, explain with neat Input and output waveforms for negative Clamping circuit. [10]

Ans.: Sometimes it is necessary to add a dc level to the ac signal. The circuits which are used to add dc level as per the requirement into the signal ac are known as Clamper Circuits. The capacitor, diode and the resistor are the 3 basic elements of the clamper circuits. The clamper circuit is also known as dc restorer (or) dc insertor circuit.

Depending upon whether the positive d.c. (or) negative dc shift is to be introduced, clampers are classified into two types :

1. Positive Clamper
2. Negative Clamper



1. The simple positive clamper circuit using capacitor C, diode D and load resistor R_L is as shown in figure. The circuit is used to add positive level to the ac output voltage V_o.

The operation of the circuit can be explained as follows :

Consider the first negative half cycle, during which diode D becomes forward biased and starts conducting. Hence, capacitor C starts charging through diode D and it gets charged almost equal to V_m–0.7V with the polarity as shown in figure.

Just after the negative peak, the diode becomes reverse biased and capacitor remains charged to a value V_m–0.7 with the same polarity. Now capacitor can discharge through load resistor R_L. But the value of the R_L is selected on the higher side such that the discharging time constant RLC is so large that capacitor discharges very little which can

be neglected. For a good clamper circuit RLC Time constant should be ten times the time period of input signal.

Hence the output voltage is given as :

$$V_o = V_i + V_c$$

But $V_c = V_m - 0.7$

$$\therefore \quad V_o = V_i + V_m - 0.7$$

Let $V_i = V_m$, then the V_o gets,

$$V_o = 2V_m - 0.7$$

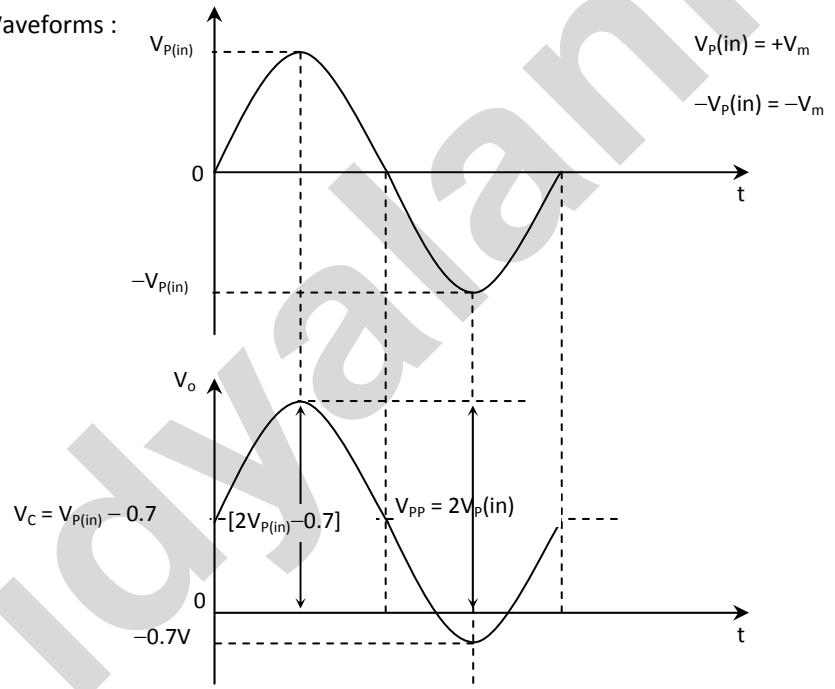
Let $V_i = 0$, then $V_o = V_m - 0.7$

Let $V_i = -V_m$, then $V_o = -0.7$

This indicates that output voltage is equal to sum of V_i and dc level of capacitor C.

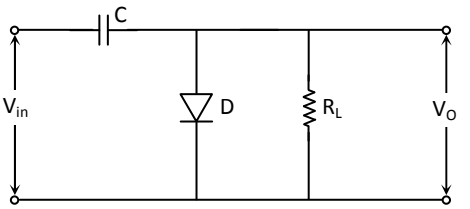
The figure shows the input and output waveform for positive clamper. It can be observed that, peak to peak value of the output is same as peak to peak value of the input signal. Only difference is that a positive dc level is added into the output signal.

Waveforms :



The figure shows the circuit diagram of negative clamper. It is a circuit which adds negative dc level to the ac output voltage. The operation of the circuit can be explained as follows:

During the positive half cycle, diode becomes forward biased and strats conducting. Therefore, current flows through the circuit and charges the capacitor upto the value $V_m - 0.7$ with the polarity as shown in figure.



Once the capacitor charges to V_m–0.7 then diode becomes reverse biased and acts as an open circuit. Now capacitor can discharge through R_L, but value of R_L is selected so high that the time constant RLC is very large and capacitor discharges very little which can be neglected.

Now when diode is acting as a reverse biased then output voltage is given as :

$V_o = V_i - V_c$ where $V_c = V_m - 0.7$

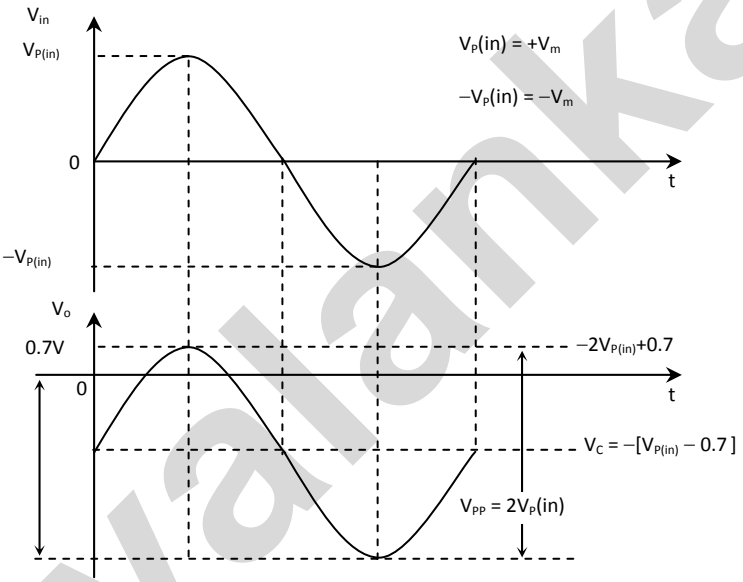
$\therefore$ $V_o = V_i - V_m + 0.7$

Let $V_i = 0$, then $V_o = -V_m + 0.7$

Let $V_i = V_m$, then $V_o = +0.7$

Let $V_i = -V_m$, then $V_o = -2\,V_m + 0.7$

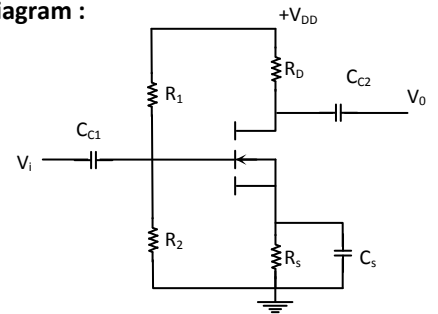
Waveform :



This indicates that output voltage is $V_m - 0.7$ dc level of ac. The circuit adds negative dc level in the signal. Hence, it is called as Negative Clamper. In this circuit also, peak to peak voltage of the output is same as the input.

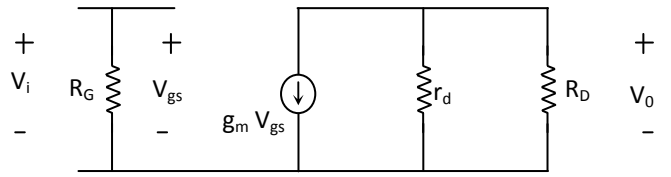
Q.6(a) For the voltage divider biased E MOSFET circuit derive equation of Input Resistance, Voltage gain and output resistance for CS amplifier. [10]

Ans.: (a) Circuit diagram :



(b) a.c. equivalent circuit : Short V_{DD} and short all capacitor.

Replace FET by its equivalent :



(d) To find voltage gain $A_V = V_0/V_i$:

$V_0 = -g_m \cdot V_{gs} \cdot (r_d \,||\, R_D)$

$V_i = V_{gs}$

$$A_V = \frac{V_0}{V_i} = \frac{-g_m V_{gs}(r_d \,||\, R_D)}{V_{gs}}$$

If R_L is connected at the output, then

$$A_{v_L} = -g_m(r_d \,||\, R_D \,||\, R_L)$$

(e) To find R_i :

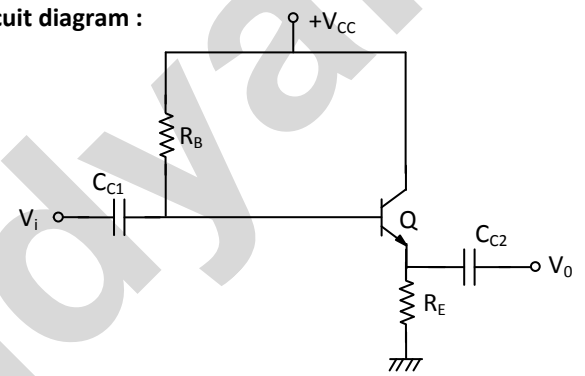
$R_i = R_G$

(f) To Find output impedance R_0 :

$R_0 = r_d \,||\, R_D$

Q.6(b) Derive equation of Input resistance, Current gain and Voltage gain for CC amplifier. [10]

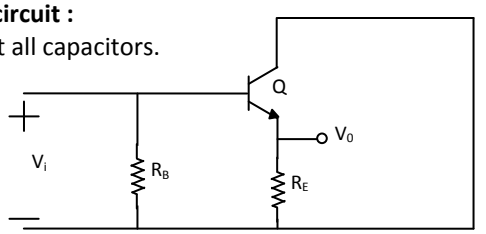
Ans.: (a) Circuit diagram :



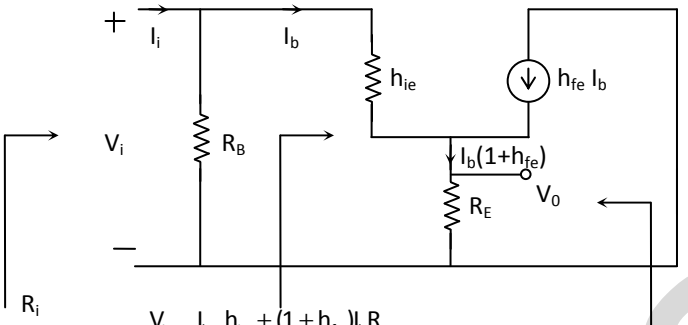
Since output is taken from emitter, emitter voltage follows the base voltage and hence the name emitter follower.

(b) ac Equivalent circuit :

Short V_{CC}, short all capacitors.



(c) Replace transistor by its equivalent :



$$\frac{V_i}{I_b} = \frac{I_b\,.h_{ie} + (1+h_{fe})I_bR_E}{I_b}$$

$$= h_{ie} + (1+h_{fe})R_E$$

(d) To find input resistance $R_i = V_i/I_i$:

$$= \frac{\left[h_{ie} + (1+h_{fe})R_E\right].R_B}{R_B + h_{ie} + (1+h_{fe})R_E} = R_B \,||\left[h_{ie} + (1+h_{fe})R_E\right]$$

(e) To find output resistance R_0 :

$$R_0 = \frac{h_{ie}}{1+h_{fe}} \,||R_E = \frac{1}{g_m}||R_E$$

(f) To find voltage gain $A_v = V_0 / V_i$:

$$A_v = \frac{\text{Output Voltage } (V_0)}{\text{Input Voltage } (V_i)} = \frac{I_b(1+h_{fe}).R_E}{I_b.\left[h_{ie} + (1+h_{fe})R_E\right]} = \frac{(1+h_{fe})R_E}{h_{ie} + (1+h_{fe})R_E}$$

(g) To find current gain $A_I = I_0 / I_i$:

$$A_i = \frac{\text{output current}}{\text{input current}} = \frac{I_0}{I_i} = \frac{I_0}{I_b}.\frac{I_b}{I_i}$$

$$= \frac{(1+h_{fe})I_b}{I_b}.\frac{R_B}{R_B + h_{ie} + (1+h_{fe})R_E} = \frac{(1+h_{fe}).R_B}{R_B + h_{ie} + (1+h_{fe})R_E}$$

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