Prelim Paper **Digital System Design**

Time: 3 Hrs.] **[Marks : 80**

N.B.: (1) Question number 1 is compulsory.
(2) Solve any three questions from the remaining five.
(3) Figure to the right indicates full marks.
(4) Assume suitable data if required and mention it in answer sheet.

1. Solve following : **[20]**
(a) Explain the following decimals in gray code form
(i) $(42)_{10}$ (ii) $(17)_{10}$
(b) Design a full adder using 3:8 Decoder
(c) Convert JK flip flop to T flip flop.
(d) Perform the following operation using 2's compliment
(i) $(7)_{10} - (15)_{10}$ (ii) $(50)_{10} - (2A)_{16}$
Comment on results of (i) and (ii)

2. (a) Prove that NAND and NOR gates are Universal gates. **[10]**
(b) Design 3 bit Binary to gray code Converter **[10]**

3. (a) Minimize the following expression using Quine Mc–cluskey technique. **[10]**
$F(A,B,C,D)=\Sigma(0,1,2,3,5,7,9,11)$
(b) What are shift registers? How are they classified? Explain working of any one type of shift register. **[10]**

4. (a) Design a 2 bit comparator and implement using logic gates **[10]**
(b) Explain Master slave JK Flip flop **[5]**
(c) Convert T flip flop to D flip flop. **[5]**

5. (a) What is shift register? Explain any one type of shift register. Give its applications. **[10]**
(b) Explain Full Adder circuit using PLA having three inputs, 8 product terms and two outputs. **[10]**

6. Explain the following : **[20]**
(a) VHDL Code for Full Subtractor.
(b) Explain SRAM and DRAM.
(c) Compare TTL and CMOS logic families.
(d) Explain CPLD and FPGA.

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