S.E. Sem. III [EXTC]

Electronic Devices and Circuits I

Time : 3 Hrs.] Prelim Paper Solution **[Marks : 80**

Q.1 Attempt any FIVE questions :

Q.1(a) Explain various types of resistors. **[5]**

Ans.: There are two basic types of resistors.

1. Linear Resistors
2. Non Linear Resistors

Linear Resistors :

Those resistors, which values change with the applied voltage and temperature, are called linear resistors. In other words, a resistor, which current value is directly proportional to the applied voltage is known as linear resistors.

Generally, there are two types of resistors which have linear properties.

(a) Fixed Resistors (b) Variable Resistors

(a) Fixed Resistors : As the name tells everything, fixed resistor is a resistor which has a specific value and we can't change the value of fixed resistors.

Types of Fixed resistors :

- Carbon Composition Resistors
- Wire Wound Resistors
- Thin Film Resistors

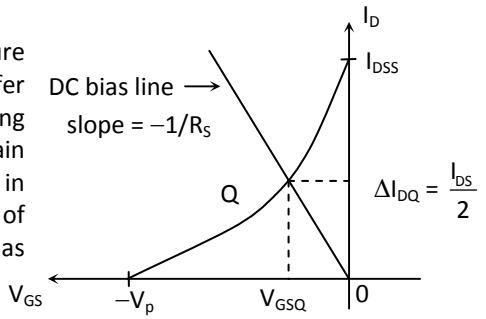
Q.1(b) Why gain of BJT is higher than gain of JFET? **[5]**

Ans.: Gain of BJT is proportional to β and β is large hence gain of BJT is large, whereas gain of FET is proportional to g_m and is of order of milli, hence gain of JFET is small.

Q.1(c) What is zero temperature drift biasing. **[5]**

Ans.: Mutual Characteristics of JFET

The operation of JFET is temperature dependent. Hence, when we plot the transfer characteristics of JFET for different operating temperatures, it can be seen that the drain current I_D decreases with increase in temperature. The transfer characteristics of JFET for different operating temperature is as shown.



Assume $T_3 > T_2 > T_1$. One of the important characteristics of JFET is, all the transfer characteristics cross a particular point on the transfer curve. If this point is selected as the operating point of JFET, it can be seen that the drain current I_{DQ} is independent of temperature. This phenomenon by which I_{DQ} is made independent of temperature is called Zero Temperature Drift. The condition for Zero Temperature Drift is $|V_p| - |V_{GS}| = 0.63$ volts.

Effect of temperature on mutual characteristics

There are two factors associated with zero temperature drift.

1) When temperature increases, the lattice atoms gains energy, they vibrate faster, hence collisions between the lattice atom and the carrier increases. Due to increased number of collisions, the mobility of the carrier decreases. Hence I_D decreases with increase in temperature. Experimentally it is seen that I_D decreases by 0.7 % of I_D.

$$\therefore \quad \Delta I_D = 0.007\, I_D \qquad \ldots (1)$$

2) When temperature increases, the junction barrier decreases. The decrease in junction barrier increases the width of the channel, hence the resistance offered by the channel decreases, hence I_D increases. Experimentally it is seen that the increase in I_D is proportional to 2.2 mV change in V_{GS} per °C.

$$\therefore \quad \Delta I_D = g_m \Delta V_{GS}$$
$$= 2.2 \times 10^{-3}\, g_m \qquad \ldots (2)$$

At one point on the transfer curve, the decrease in I_D due to decrease in mobility and increase in I_D due to decrease in junction barrier will oppose each other, making the drain current independent of temperature. This is the principle behind zero thermal drift.

Q.1(d) Consider a BJT has parameters f_T = 500 MHz at I_C = 1mA, β = 100 and $C\mu$ = 0.3 pF. Calculate bandwidth of f_β and capacitance C_π of a BJT. **[5]**

Ans.: Given : f_T = 500 MHz at I_C = 1mA, β = 100 and $C\mu$ = 0.3 pF

Find : f_β, C_π

$f_T = \beta\, f_\beta$

$\therefore \quad f_\beta = 5$ MHz

$$r_e = \frac{26\text{mV}}{I_C} = 26$$

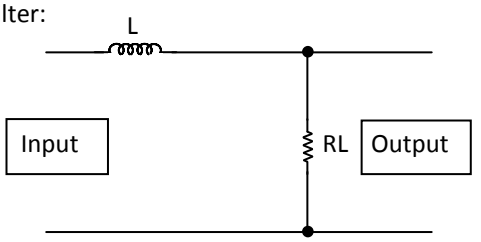
$\therefore \quad h_{ie} = \beta\, r_e = 2.6\ \text{k}\Omega$

$$f_\beta = \frac{1}{2\pi h_{ie}(C_\pi + C_\mu)} = \frac{1}{2\pi(2.6\text{k})(C_\pi + C_\mu)}$$

$C_\pi = 11.9$ Rf

Q.1(e) Write short note on different types of filters. **[5]**

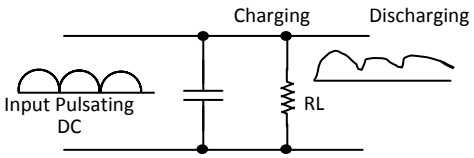
Ans.: (i) Inductor Filter:



This type of filter is also called choke filter. It consists of an inductor L which is inserted between the rectifier and the load resistance. R_L. The rectifier contains A.C components as well as D.C components. When the output passes through the inductor, it offers a high resistance to the A.C component and no resistance to D.C components. Therefore,

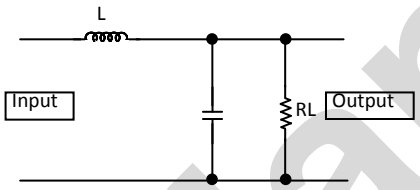
A.C components of the rectified output is blocked and only D.C components reached at the load.

(ii) Capacitor Filter:



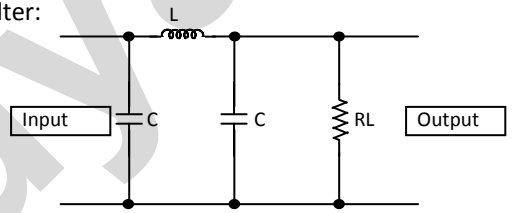
In this filter a capacitor is connected across the load during the rise of voltage cycle it gets charge and this charge is supply to the load during the fall in the voltage cycle. This process is repeated for each cycle and thus the repel is reduced across the load. It is shown in the above Figure. It is popular, because of its low cost. Small size, less weight and good characteristics. Useful for load up to 50mA as in transistor radio battery eliminators.

(iii) LC Filter:



In inductor filter, the ripple factor is directly proportional to the load resistance. On the other hand in a capacitor filter, it is varying inversely with the load resistance. Hence if we combine the inductor filter with the capacitor the ripple factor will become almost independent of the load filter. It is also known as inductor input filter, choke input filter. L input or LC-section.

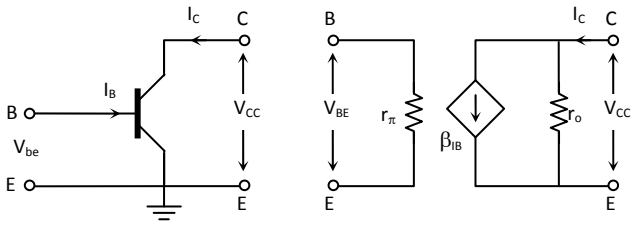
(iv) CLC or Pie Filter:



It consists of one inductor and two capacitor connected across its each end. The three components are arranged in shape of Greek letter Pi. It is also called capacitor input Pi filter. The input capacitor C_1 is selected to offer very low reactance to the repel frequency hence major parts of filtering is done by C_1. Most of the remaining repels are removed by the combining action of L and C_2. This circuit gives much better filter then LC filter. However C_1 is still directly connected across the supply and would need high pulse of current if load current is large. This filter is used for the low current equipment's.

Q.1(f) Explain the hybrid pi model of BJT. **[5]**

Ans.:



The figure shows hybrid model of a BJT in which :

(i) r_π = It is the resistance offered by forward biased BE junction, given as,

$$r_\pi = \frac{\beta VT}{I_{CQ}}$$

β : forward current gain, VT : 26 mV, I_{CQ} : DC value of collector current.

(ii) The β_{IB} is a dependent current source which indicates the collector current of BJT.

(iii) As we known that in, BJT we have early effect, because BJT offers finite value of output resistance r_o, given as :

$$r_o = \frac{V_A}{I_{CQ}}$$

V_A : Early voltage of BJT, I_{CQ} : DC value of collector current

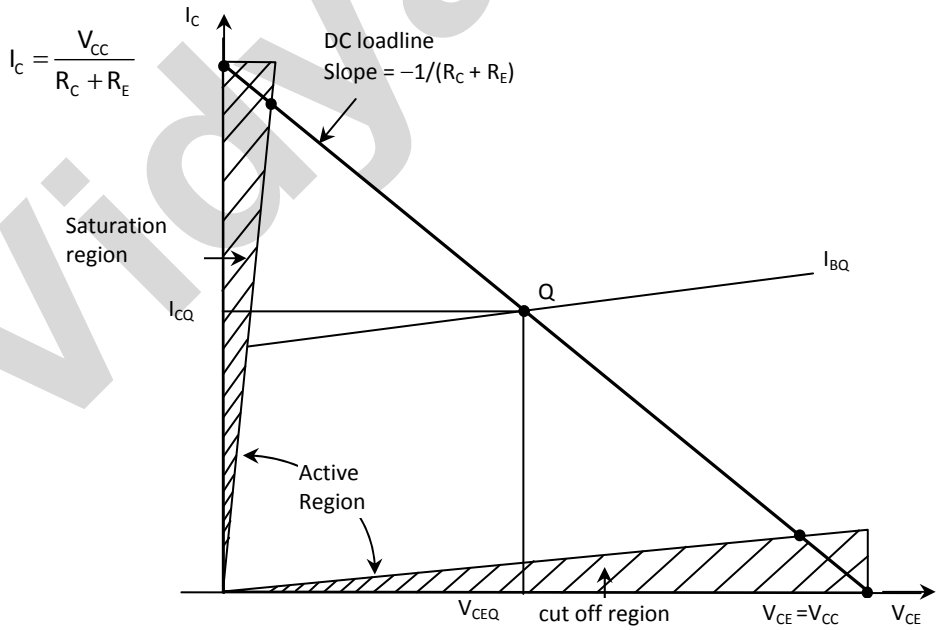
(iv) g_m is known as transconductance of BJT is given as :

$$g_m = \frac{I_{CQ}}{V_A}$$

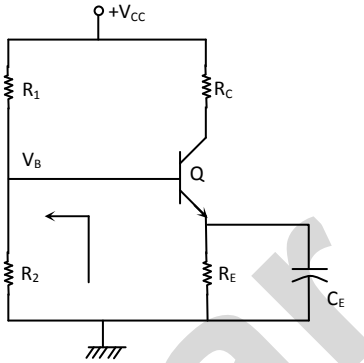
Q.2(a) Write short note on DC load line and significance of Q-point **[10]**

Ans.: Concept of DC Loadline :

Consider the output characteristics of CE transistor as shown



Consider a fixed bias or self bias or voltage divider bias circuit using transistor.



Apply KVL to the collector side,

$V_{CC} = I_C R_C + V_{CE} + (I_C + I_B) R_E$

$V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E$

$\approx V_{CC} - I_C (R_C + R_E)$

$\therefore I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$

This equation is of the form y = mx + c, an equation to a straight line having slope = $-\left(\frac{1}{R_C + R_E}\right)$ and having y intercept = $\frac{V_{CC}}{R_C + R_E}$ and x intercept = V_{CC}.

This line is called DC loadline. It will intercept the output characteristics for a given value of I_B at a point called Q point.

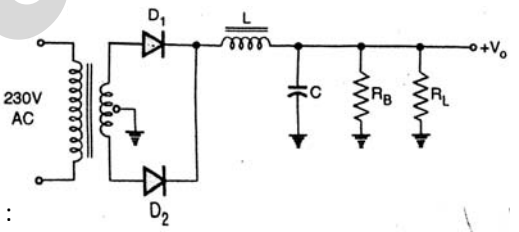
The significance of DC load line is that it actually indicates region of operation.
if it is to be operated s switch then Q point should be chosen in saturation of cutoff region and if it is to be operated as an amplifier then it should be operated in Active region.

Q.2(b) A full wave rectifier using a center tapped transformer with two diodes gives output voltage of 250 V to a resistive load, the current being 75 ± 25 mA. If the ripple factor is 0.001, calculate the specification of the devices and components required fi the filter used are L section LC filter. **[10]**

Ans.: V_{Ldc} = 250 V, I_{Ldc} = 75 ± 25 mA, r = 0.001

L section (LC) filter :

- Circuit diagram :



- Range of the load resistance :

$R_{L(min)} = \frac{V_{Ldc}}{I_{L(max)}} = \frac{250}{100 \times 10^{-3}} = 2.5\ k\Omega$

$R_{L(max)} = \frac{V_{Ldc}}{I_{L(min)}} = \frac{250}{75 \times 10^{-3}} = 3.3\ k\Omega$

$\therefore$ $R_{L(min)}$ = 2.5 kΩ and $R_{L(max)}$ = 3.3 kΩ

- Value of LC :
  To ripple factor is given by

$r = \frac{1}{6\sqrt{2}\,\omega^2 LC}$

with f = 50 Hz, r = 0.001 we have

$$LC = \frac{1}{6\sqrt{2}\,\omega^2 r} = \frac{1}{6\sqrt{2}\,(2\pi\times 50)^2\times 0.001} = 1.194\times 10^{-3}$$

- **Bleeder resistance R_B :**

Let us assume bleeder current to be 10% of maximum current,

Bleeder current, $I_B = 0.1 \times$ Maximum load current

$= 0.1 \times 100$ mA $= 10$ mA

Bleeder resistor, $R_B = \frac{V_{Ldc}}{\text{Bleeder current}} = \frac{V_{Ldc}}{I_B}$

$$\therefore \quad R_B = \frac{250}{10\text{mA}} = 25\ \text{k}\Omega$$

Wattage of R_B,

$W_{Rb} \geq V_{Ldc} \times I_B = 250 \times 10 \times 10^{-3} \geq 2.5$ W

Select R_B = 25 kΩ/5 W

- **Calculate L_C and select L :**

Critical inductance, $L_C = \frac{R_B}{3\omega} = \frac{25\times 10^3}{3\times 2\pi\times 50} = 26.5$ H

Select L = 30 H, 100 mA

- **Calculate C :**

We have, $LC = 1.194\times 10^{-3}$

$$\therefore \quad C = \frac{1.194\times 10^{-3}}{30} = 3.98\times 10^{-5}\ \text{F}$$

$$\therefore \quad C = 39.8\ \mu\text{F}$$

Select, C = 47 μF/500 V

- **Ratings of the diodes :**

Average current through diode $= \frac{I_{Ldc}+I_b}{2} = \frac{100+10}{2} = 55$ mA

$$\therefore \quad I_{avg} = 55\ \text{mA}$$

The load voltage is the voltage across capacitor C which charges to V_m Volts. With a very small value of 'r', the ripple voltage is small.

$$\therefore \quad V_{Ldc} = V_m = 250\ \text{V}$$

PIV of each diode, V_m = 250 V

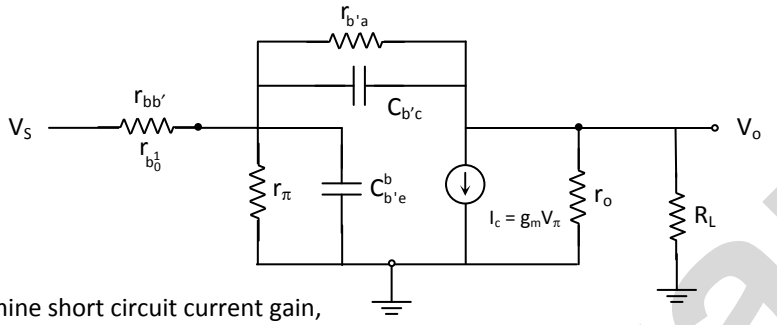
- **Ratings of transformer :**

Secondary rms voltage, $V_{s\,(rms)} = \frac{V_m}{\sqrt{2}} = \frac{250}{\sqrt{2}} = 176.7$ V

$$\therefore \quad \text{Turns ratio, } \frac{N_1}{N_2} = \frac{230}{176.7} = 1.3$$

Q.3(a) Obtain expression for gain bandwidth product. **[10]**

Ans.: The small signal high frequency π–model of CE amplifier with load is as shown :



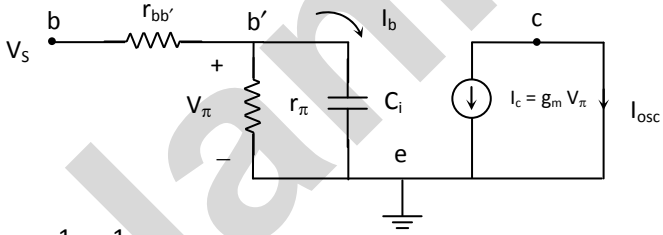
To determine short circuit current gain,

$A_{isc} = \frac{I_{OSC}}{I_B}$, short the load.

The resulting model is as shown,

$\rightarrow r_{\pi(k\Omega)} \,||\, r_{b'c\,(M\,\Omega)} \approx r_{\pi\,(k\Omega)}$

$\rightarrow C_{b'e} + C_{b'c} = C_i$



$$A_{isc} = \frac{I_{OSC}}{I_b}$$

$$\therefore \quad I_{OSC} = -g_m \,.\, V_\pi$$

$$\therefore \quad V_\pi = I_b \,.\, Z = \frac{I_b}{y}$$

$$Z = \left(r_\pi \,||\, \frac{1}{s_{ci}} \right) \qquad \therefore \quad \frac{1}{Z} = \frac{1}{r_\pi} + S_{Ci}$$

$$\therefore \quad y = gm_\pi + S_{Ci}$$

$$\therefore \quad V_\pi = \frac{I_b}{g_{m\pi} + S_{Ci}}$$

$$\therefore \quad I_{OSC} = -g_m \,.\, \frac{I_b}{g_{m_\pi} + S_{Ci}}$$

$$\therefore \quad A_{isc} = \frac{I_{OSC}}{I_b} = \frac{-g_m}{g_{m_\pi} + S_{Ci}}$$

$$\therefore \quad A_{isc} = \frac{-g_m}{g_{m_\pi}\left[1 + \frac{S_{Ci}}{g_{m_\pi}}\right]}$$

$$\therefore \quad A_{isc} = \frac{-g_m \,.\, r_\pi}{1 + j\left(\frac{f}{f_\beta}\right)} \quad \text{.....where } f_\beta = \frac{1}{2\pi r_\pi C_i}$$

$$r_\pi = h_{ie} = h_{fe} \,.\, r_e = \frac{\beta}{g_m} \qquad \beta = r_\pi \,.\, g_m$$

$\therefore \quad A_{isc} = \dfrac{-\beta}{1 + j\left(\dfrac{f}{f_\beta}\right)}$

$f_\beta = \dfrac{1}{2\pi h_{ie}\,[C_{be} + C_{bc}]}$

$|x \pm jy| = \sqrt{x^2 + y^2}$

$|A_{isc}| = \dfrac{\beta}{\sqrt{1 + \left(\dfrac{f}{f_\beta}\right)^2}}$

Case 1: $f < f_\beta \ \therefore \quad \dfrac{f}{f_\beta} < 1 \quad \therefore \quad \left(\dfrac{f}{f_\beta}\right)^2 << 1$ (neglect)

$|A_{isc}| = \beta =$ constant

$\rightarrow$ Pass Band, i.e. gain in pass band remains constant.

Case 2: $f = f_\beta$ (cut–off frequency)

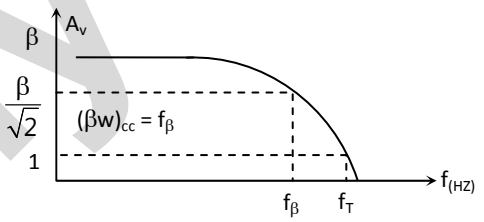
$A_{isc} = \dfrac{\beta}{\sqrt{2}}$

Case 3: $f > f_\beta \qquad \therefore \quad \left(\dfrac{f}{f_\beta}\right)^2 >> > 1$

$\therefore |A_{isc}| = \dfrac{\beta}{\sqrt{\left(\dfrac{f}{f_\beta}\right)^2}} = f_\beta \cdot \dfrac{\beta}{f} \Rightarrow |A_{isc}| \propto \dfrac{1}{f}$

$\rightarrow$ In stop band as frequency increases , gain decreases

From (1), (2) and (3), the responses are shown :



$\because$ lower cut–off frequency is negligible compared to upper cut–off (f_β)

$\therefore$ B_w = upper cut–off (f_β)

The frequency at which amplifier provides unit gain.

i.e. $|A_{isc}| = 1$

$\rightarrow$ At $f = f_T \quad |A_{isc}| = 1$

From equation (1)

$\therefore$ From graph, $f_T > f_\beta \qquad \therefore \quad \dfrac{f_T}{f_\beta} > 1$

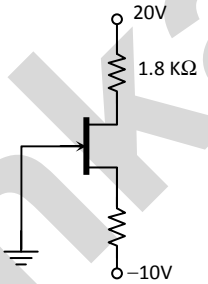
$\therefore \quad \left(\frac{f_T}{f_\beta}\right)^2 >>> 1$ neglect 1

$\therefore \quad 1 = \frac{\beta}{\sqrt{\left(\frac{f_T}{f_\beta}\right)^2}} \Rightarrow \frac{f_T}{f_\beta} = \beta \quad \therefore \quad f_T = \beta . f_\beta$

$\therefore \quad f_T$ = Gain × BW
= Gain − BW Product

And Gain − BW Product (GBP) for an amplifier always remains constant.

Q.3(b) Determine I_{DQ}, V_{GSQ}, V_{DSQ} if I_{DSS} = 9 mA and V_p = –3V for the circuit given in Figure. **[10]**



Ans.: I_{DSS} = 9 mA, $V_P = -3V$

KVL at gate,

$0 - V_{gs} - I_D R_S + 10 = 0$

$V_{gs} = 10 - I_D$

$V_{gs} = +0.14$ V

$I_D = I_{DSS}\left[1 - \frac{V_{gs}}{V_P}\right]^2 = 9\left[1 - \frac{10 - I_D}{3}\right]^2$

= 9.85 mA

$V_{DS} = V_{DD} - I_D = -7.58$ V

Q.4(a) Design single stage BJT CE Amplifier for the following requirements. **[15]**
$A_V \geq 100$, $Z_i \geq 3K\Omega$, V_{CC} = 18 V

Ans.: Given : $A_V \geq 100$, $Z_i \geq 3K\Omega$, V_{CC} = 18 V

Selection of transistor : We select BC1478 with following parameters,

$P_{D\,max}$ = 0.25 W, $I_{C\,max}$ = 0.1 A, V_{CEO} = 48V, h_{fe} = 330, h_{ie} = 4.5 kΩ,
V_{BE} = 0.7 V, $V_{CE\,out}$ = 0.25 V

Selection of bias : We use voltage divider bias with R_E partially by passed.

Design of R_C : Let R_C = 10 kΩ

$|A_V| = \frac{h_{fe} R_C}{h_{ie} + (1 + h_{fe}) R_{E1}}$

Let R_{E1} = 100 Ω; (1/4)W

R'_C = 1253 kΩ $= \frac{R_C R_C}{R_C + R_C}$

R_C = 1.432 kΩ

$R_{C\,sat}$ = 1.5 kΩ; (1/4)W

To determine Q point :

$V_{CEQ} = \frac{V_Q}{2}$ (mid point bias)

$= 9V$

Let $V_{RE} = 10\%$, $V_{CC} = 1.8$ V

$I_C = \frac{V_{CC} - V_{CE} - V_{RE}}{R_C} = 4.8$ mA

$\therefore \quad V_{CEQ} = 9V, \; I_{CQ} = 4.8$ mA

Determine of R_E,

$V_{RE} = 1.8 = I_C R_E$

$R_E = \frac{V_{RE}}{I_C} = 375\ \Omega$

but $R_E = R_{E1} + R_{E2}$

$\therefore \quad R_{E2} = 275\ \Omega$

$R_{E2} = 270\ \Omega$; (1/4)W

To design R_1 and R_2,

Given, $R_i = 3\ k\Omega$, Let $R_i = 3.2\ k\Omega$

but $R_i = R_B \,||\, (h_{ie} + (1 + h_{fe}) R_{E1})$

$3.2k = \frac{R_B\, y}{R_B + y}$ $\qquad y = h_{ie} + (1 + h_{fe}) R_{E1} = 37.6\ k\Omega$

$R_3 = 3.497\ k\Omega = \frac{R_1 R_2}{R_1 + R_2}$

$V_B = V_{BE} + V_{RE} = 0.7 + 1.8 = 2.5$ V

$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$

$\therefore \quad \frac{R_3}{R_1 + R_2} = \frac{V_B}{V_{CC}} = 0.1388$

$R_1 = 25.178\ k\Omega$

$R_2 = 4.057\ k\Omega$

$R_{1\,sat} = 27\ k\Omega$; (1/4)W

$R_{2\,sat} = 3.9\ k\Omega$; (1/4)W

Design of capacitors :

Let f = 20 Hz

$f_{LCC1} = \frac{1}{2\pi R_i C_{C1}}$

$R_i = R_B \,||\, (h_{ie} + (1 + h_{fe}) R_{E1}) = 252\ k\Omega$

$C_{C1} = 2.4\ \mu F$

Let $C_{C1} = 10\ \mu F$; 5V

$$f_{LCC2} = \frac{1}{2\pi R_0 C_{C2}} \qquad R_0 = R_C + R_E = 11.5\ k\Omega$$

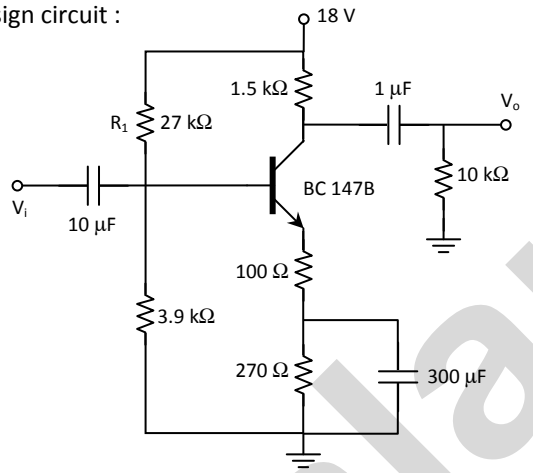
C_{C2} = 0.7 μF

C_{C2} = 1 μF ; 20V

$$f_{LCC} = \frac{10}{2\pi R_{E2} C_E} \qquad C_E = 294\ \mu F$$

C_C = 300 μF; 5V

Design circuit :



Q.4(b) For above designed circuit calculate A_v, R_i, and R_o. **[5]**

Ans.: From Q.4(a) design circuit,

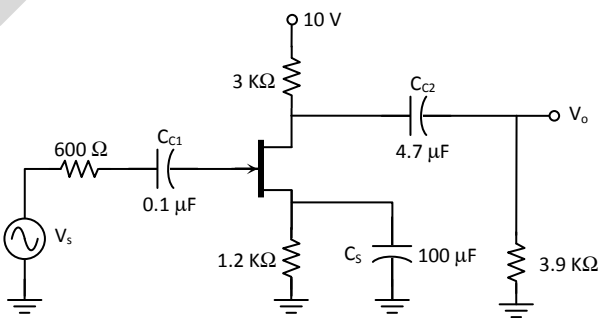
$R_o = R'_C = R_C \,||\, R_E = 1.253\ k\Omega$

$$A_V = \frac{-h_{fe} R'_C}{h_{ie} + (1 + h_{fe}) R_{C1}} = 10.9$$

$R_i = R_B \,||\, [h_{ie} + (1 + h_{fe})\, R_{CC1}]$

R_i = 3.2 kΩ

Q.5(a) For the circuit using JFET as shown in Figure, if I_{DSS} = 6 mA, V_P = –6V, r_d = ∞, C_{gd} = 4 pF, C_{gs} = 6 pF, C_{ds} = 1 pF, determine : higher cutoff frequency. **[10]**



Ans.: Given : $I_{DSS} = 6$ mA, $V_P = -6$V, $r_d = \infty$, $C_{gd} = 4$ pF, $C_{gs} = 6$ pF, $C_{ds} = 1$ pF

$V_{gs} = -I_D R_s = -1.2 I_D$

$= -2.4$V

$$I_D = I_{DSS}\left[1-\frac{V_{gs}}{V_p}\right]^2 = 2.1 \text{ mA}$$

$$g_m = \frac{I_{DSS}}{|V_P|}\left[1-\frac{V_{gs}}{V_P}\right] = 1.31 \text{ m℧}$$

$|A_V| = g_m R'_D \Rightarrow R'_D = 3\text{ k}\Omega \,||\, 3.9\text{ k}\Omega = 1.09$ k

$|A_V| = 2.22$

$$\left|\frac{A_V}{\sqrt{2}}\right| = 1.57$$

$R_i = 600\ \Omega$

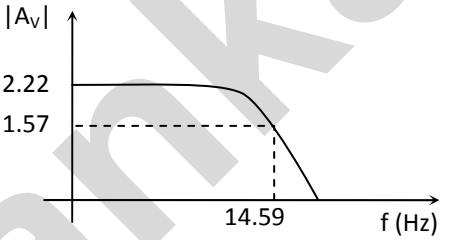
$C_i = C_{gs} + (1 + A) C_{gd} = 18.88$ Rf

$$f_{HC} = \frac{1}{2\pi R_i C_i} = 14.05 \text{ MHz}$$

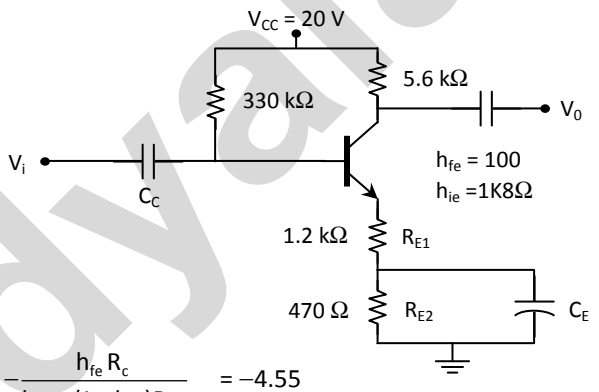
$R_o = R_D \,||\, R_2 = 1.69\text{ k}\Omega$

$C_o = C_{ds} + C_{mo} = 5$ pF

$f_{HC} = 18$ kHz



Q.5(b) Find Z_0, Z_i, A_V, A_i for the network given : [10]



Ans.: $$A_V = -\frac{h_{fe} R_c}{h_{ie} + (1 + h_{fe}) R_{E1}} = -4.55$$

$$A_i = -h_{fc} \frac{R_3}{R_3 + h_{ie} + (h + h_{fe}) R_{E1}} = -100\ (0.72) = -72$$

$Z_i = R_B \,||\, (h_{ie} + (1 + h_{ie})\, R_{E1}) = 89.6\text{ k}\Omega$

$R_0 = R_C = 5.6\text{ k}\Omega$

Q.6 Write short notes on (any FOUR) : [20]

Q.6(a) Write short note on Millers Theorem. [5]

Ans.: Statement : It states that, when impedance Z is connected between input and output of an amplifier that provides gain A_v, then equivalent circuit is obtained by connecting Z_{mi} (miller's i/p impedance) at input and Z_{mo} (miller's o/p impedance) at output.

i.e.

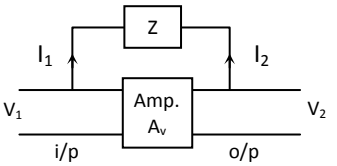


Fig. : (1)

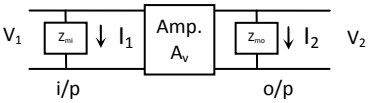


Fig. : (2)

From fig. (1)

$$I_1 = \frac{V_1 - V_2}{Z}$$

From fig. (2)

$$I_1 = \frac{V_1}{Z_{mi}}$$

Equating....

$$\frac{V_1}{Z_{mi}} = \frac{V_1 - V_2}{Z}$$

$$\therefore \frac{Z}{Z_{mi}} = \frac{V_1 - V_2}{V_1} = 1 - \frac{V_2}{V_1}$$

$$\therefore \frac{Z}{Z_{mi}} = 1 - A_v$$

$$\therefore Z_{mi} = \frac{1}{1 - A_v}.Z$$

$\Rightarrow$ For CE and CS amplifier,

a) For CE amplifier,

$$Z_{mi} = \frac{Z}{1 + |A_v|} \quad ...(1)$$

and $Z_{mo} \approx Z$ ...(2)

From fig. (1)

$$I_2 = \frac{V_2 - V_1}{Z}$$

$$I_2 = \frac{V_2}{Z_{mo}}$$

$$\frac{V_2}{Z_{mo}} = \frac{V_2 - V_1}{Z}$$

$$\therefore \frac{Z}{Z_{mo}} = 1 - \frac{V_1}{V_2}$$

$$\therefore \frac{Z}{Z_{mo}} = 1 - \frac{1}{A_v} = \frac{A_v - 1}{A_v}$$

$$\therefore z_{mo} = \frac{A_v}{A_v - 1}.Z$$

.....gain of CE is $-$(inverted) A_v

$\frac{A_v}{A_v - L}$ and A_v is very high

$A_v >>>> 1$

Q.6(b) Write short note on stability factors of various biasing techniques of BJT. [5]

Ans.: (a) Temperature stability factor S_I/S

It is defined as the ratio of the change in the collector current to the change in the leakage current, keeping β and V_{BE} constant.

$$S_I = \frac{\Delta I_C}{\Delta I_{CO}}, \quad \beta, \ V_{BE} \text{ constant.}$$

(b) Voltage stability factor S_V/S'

It is defined as the ratio of the change in the collector current to the change in the base emitter voltage keeping I_{CO} and β constant.

$$S_V = \frac{\Delta I_C}{\Delta V_{BE}}, \ I_{CO}, \beta \text{ constant.}$$

(c) β stability factor S_β /S″

It is defined as the ratio of the change in the collector current to the change in the value of β, keeping I_{CO} and V_{BE} constant.

$$S_\beta = \frac{\Delta I_C}{\Delta \beta}, \quad I_{CO}, V_{BE} \text{ constant.}$$

$\therefore$ the total change in I_C is given by

$$\Delta I_C = S_I \Delta I_{CO} + S_V \Delta V_{BE} + S_\beta \Delta \beta$$

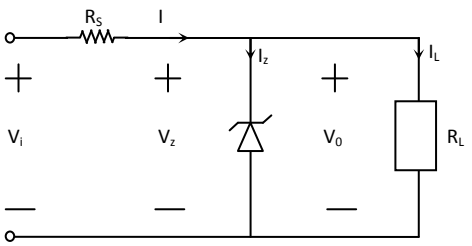
Q.6(c) Comparison of BJT CE ,CB and CC amplifier [5]

Ans.:

Mode	Type	ϕ Shift	Av	Ai	Zi/Ri
CE	Inverted	180°	$\frac{-h_{fe}.R_c}{h_{ie}} = -g_m . R_c$ large	$\beta = h_{ie}$ 20 – 500 large	$h_{ie} = \pi$ Moderate (in kΩ)
CB	Non–Inverted	0	$g_m R_c$ large	α = 0.9 – 0.99 small	$r_e = \frac{r_\pi}{\beta}$ 10 Ω – 100 Ω small
CC	Buffer	0	A_v = 1 (ideal) 0.9 – 0.99	β + 1 large	$r_\pi + (1 + \beta)R_E \infty$ (ideal)

Q.6(d) Write short note on Zener as Regulator. [5]

Ans.: The circuit diagram of zener shunt regulator is as shown. The zener is connected in shunt with the load, and zener is kept reverse biased. The unregulated input V_i must be greater than V_0 , atleast by 5 to 10 V. The resistor R_S will ensure a minimum current through zener when $V_i = V_{i\ min}$, keeping the zener in ON state. Also it limits the maximum value of zener current when $V_i = V_{i\ max}$.



In the ON state, zener maintains a constant voltage across its terminals. Therefore $V_0 = V_z$. Since V_z is a stable zener reference source, the output voltage is stable and hence the load gets a constant voltage.

Q.6(e) Write short note on JFET as VVR. [5]

Ans.: In most linear applications of field effect transistors, the device is operated in the constant current portion (Pinch–off Region) of its output characteristic. Now, consider FET operation in the region before pinch–off, where V_{DS} is small. In this region FET behaves as a voltage controlled resistor; i.e. the drain to source resistance is controlled by the bias voltage V_{GS}. In such an application the FET is also referred to as a voltage variable resistor (VVR) or voltage dependent resistors (VDR).

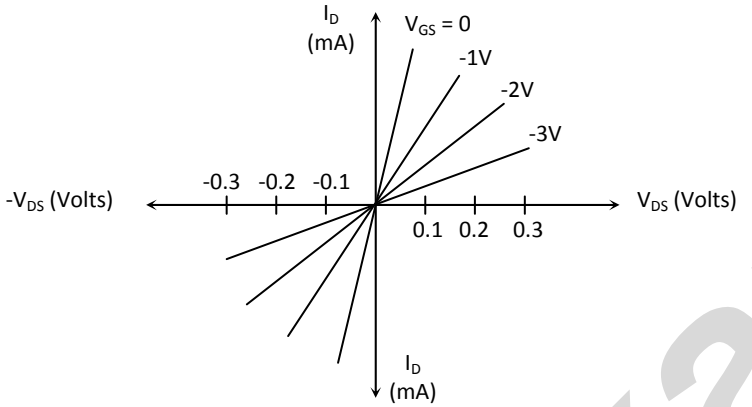


Figure above shows the low level bidirectional characteristics of JFET. The slope of these characteristics gives r_d as a function of V_{GS}. Figure drawn above has been extended into the third quadrant to give an idea of device linearity around $V_{DS} = 0$.

The variation of r_d with V_{GS} is given by, $r_d = \frac{r_0}{1 - KV_{GS}}$

where r_0 is the drain resistance at zero gate bias, K is a constant dependent upon JFET type, V_{GS} is the gate to source voltage.

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