S.E. Sem. III [INFT]

Logic Design

Prelim Paper Solution

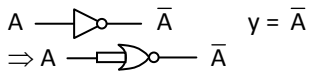
Time : 3 Hrs.] **[Marks : 80**

Q.1 Solve the following (any FOUR) : [20]

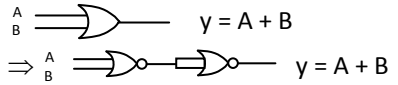
Q.1(a) Prove that NOR gate is a universal gate. [5]

Ans.: NOR gate is a universal gate because we can implement any logic gate & any Boolean expression using NOR gate only.

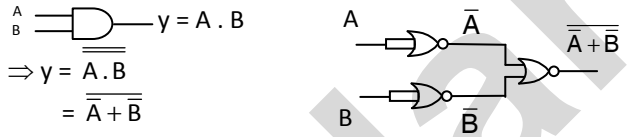
1) NOT gate using NOR



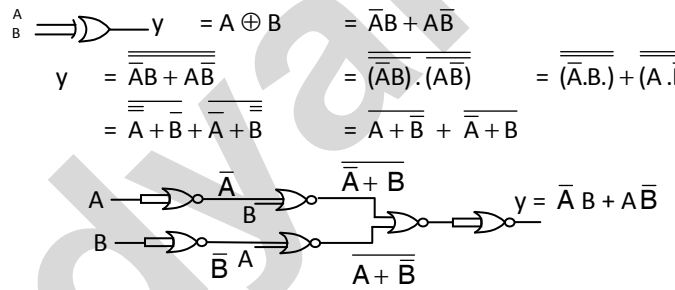
2) OR gate using NOR gate :



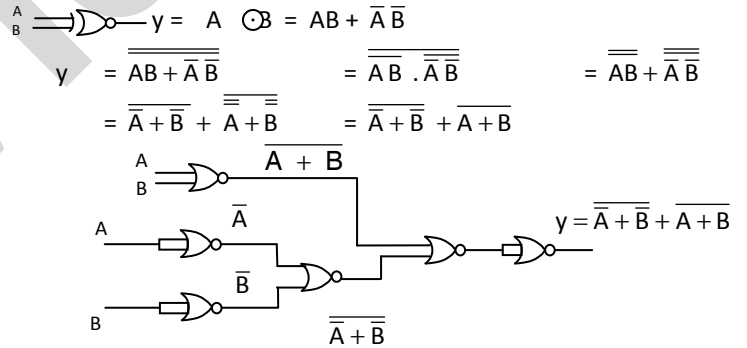
3) AND gate using NOR gate :



4) EXOR gate using NOR gate :



5) EX-NOR gate using NOR gate :



Hence we can say NOR is universal gate.

Q.1(b) Derive relation between α and β. **[5]**

Ans.: $\alpha \rightarrow$ current amplification factor for CB

$\beta \rightarrow$ current amplification factor for CE

$$\alpha = \frac{I_C}{I_E} \quad \& \quad \beta = \frac{I_C}{I_B}$$

We know, $I_E = I_C + I_B$

Divide both side by I_C

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{\beta + 1}{\beta}$$

$$\alpha = \frac{\beta}{1+\beta}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

Q.1(c) Design full adder using half adder and additional gates. **[5]**

Ans.:

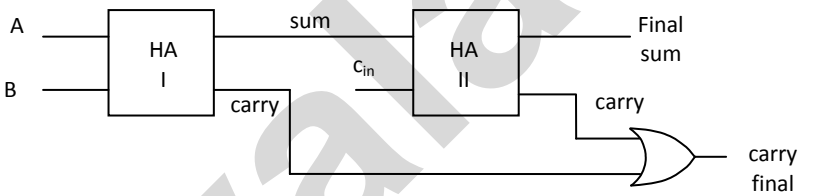


Fig. 1 : Block diagram Representation for Full Adder using Half Adder.

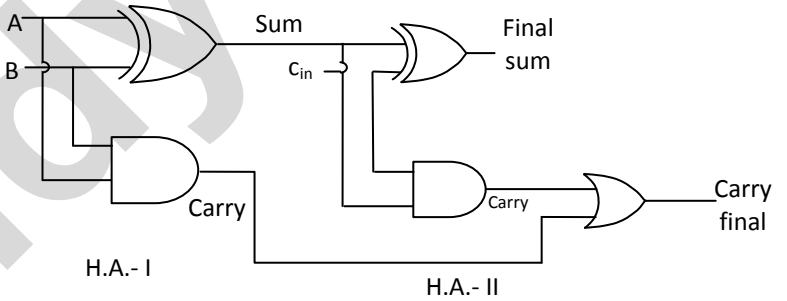
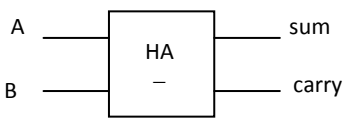
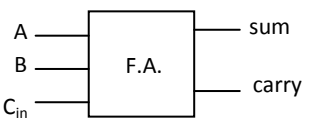


Fig. 2 : Full Adder using Half adder using Logic gates.



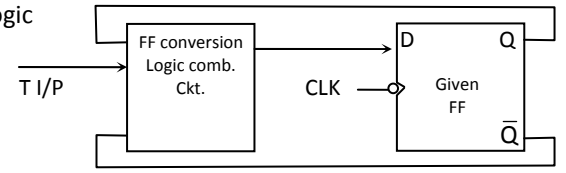
Half Adder



Full Adder

Q.1(d) Covert D flip flop to T flip flop. **[5]**

Ans.: Step I : Conversion Logic



Step II : Truth Table

T	Q_n	Q_{n+1}	D
0	0	0	0
1	0	1	1
1	1	0	0
0	1	1	1

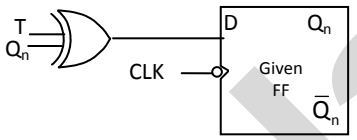
Step III : k–map for 'D'

T \ Q_n	$\overline{Q}_n$	Q_n
$\overline{T}$	0	①
T	①	0

$D = T\overline{Q}_n + \overline{T}Q_n$

$D = T \oplus Q_n$

Step IV :



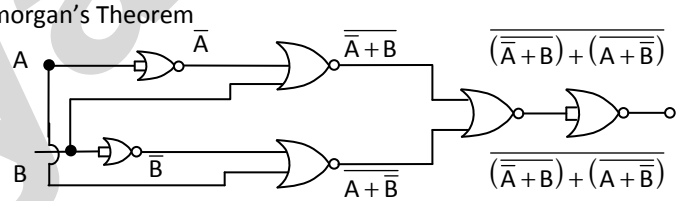
Q.1(e) Design EX-OR gate using only NOR gates. **[5]**

Ans.: $Y = A \oplus B = \overline{\overline{A\overline{B} + \overline{A}B}}$

$= \overline{(A\overline{B}).(\overline{A}B)}$ → By Demorgan's Theorem

$= \overline{(\overline{A}+B).(A+\overline{B})}$

$= \overline{(\overline{A}+B)} + \overline{(A+\overline{B})}$



Q.2(a) Using Quine Mc-Cluskey Method determine Minimal SOP form for **[10]**
f(A,B,C,D) = Σm(0,1,3,7,8,9,11,15)

Ans.: Step 1 : Grouping Minterms according to the number of '1's

Group	Minterm	Variables				Check Mark
		A	B	C	D	
0	0	0	0	0	0	
1	1	0	0	0	1	✓
	8	1	0	0	0	✓
2	3	0	0	1	1	✓
	9	1	0	0	1	✓
3	7	0	1	1	1	✓
	11	1	0	1	1	✓
4	15	1	1	1	1	✓

Step 2: Combination of Minterms Group of two

Group	Minterm	Variables				Check Mark
		A	B	C	D	
0	0,1	0	0	0	–	✓
1	1,3	0	0	–	1	✓
	1,9	–	0	0	1	✓
	8,9	1	0	0	–	
2	3,7	0	–	1	1	✓
	3,11	–	0	1	1	✓
	9,11	1	0	–	1	
3	7,15	–	1	1	1	✓
	11,15	1	–	1	1	✓

Step 3: Combination of Minterms Group of four

Group	Minterm	Variables			
		A	B	C	D
0	0,1,8,9	–	0	0	–
	0,8,1,9	–	0	0	–
1	1,3,9,11	–	0	–	1
	1,9,3,11	–	0	–	1
2	3,7,11,15	–	–	1	1
	3,11,7,15	–	–	1	1

$y = (A, B, C, D) = \overline{B}\overline{C} + \overline{B}D + CD$

Step 4 : Prime Implicant Table

PI Terms	Decimal Numbers	Minterms							
		0	1	3	7	8	9	11	15
$\overline{B}\overline{C}$	0, 1, 8, 9	⊗	x			⊗	x		
$\overline{B}D$	1, 3, 9, 11		x	x			x	x	
CD	3, 7, 11, 15			x	⊗			x	⊗

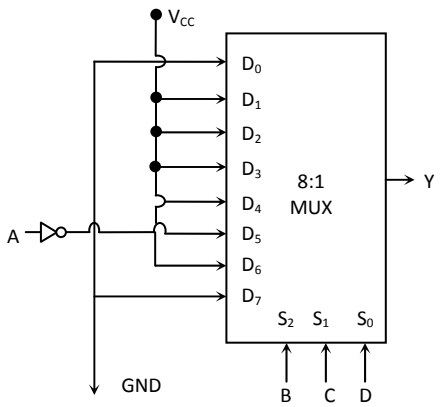
$y (A,B,C,D) = \overline{B}\overline{C} + CD$

Q.2(b) Implement following using only one 8:1 Multiplexer and few gates : [10]

$f(A,B,C,D) = \Sigma m(1,2,3,5,6,9,10,11,14)$

Ans.: $f(A, B, C, D) = \Sigma m\ (1, 2, 3, 5, 6, 9, 10, 11, 14)$

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{A}$	0	(1)	(2)	(3)	4	(5)	(6)	7
A	8	(9)	(10)	(11)	12	13	(14)	15
	0	1	1	1	0	$\overline{A}$	1	0

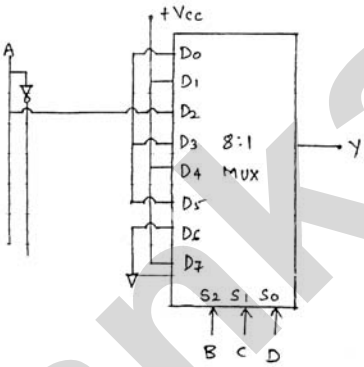


Q.3(a) With neat logic diagram explain operation of 4-bit Bidirectional Shift Register. [10]

Ans.: Step 1 : Data Table

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
⓪	①	2	③	④	⑤	6	⑦	$\overline{A}$
8	⑨	⑩	11	⑫	13	14	⑮	A
$\overline{A}$	$+V_{cc}$	A	$\overline{A}$	$+V_{cc}$	$\overline{A}$	GND	$+V_{cc}$	

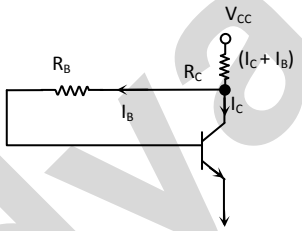
Step 2 : Implementation using MUX



Q.3(b) Explain Collector to base bias Circuit with its stability factor. [10]

Ans.: The collector to base bias circuit is an improvement over the fixed bias ckt.

- The Base resistance R_B is now connected to the collector instead of V_{CC}.
- The current flowing through R_C is the sum of I_C & I_B.



- R_B Resistor is connected as feedback element from output terminal collector to i/p terminal Base.

\# Analysis of the collector to base bias circuit:

KVL to i/p

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{(R_B + R_C) + R_C(1 + \beta_{dc})}$$

$$I_C = \beta I_B$$

KVL to output path:

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

Stability factor:

Due to change in β_{dc}, I_{co} and V_{BE} w.r.t. temp Q point of transistor gets affected. Hence we need to stabilize θpt.

$$S = \frac{\Delta I_C}{\Delta I_{CO}} = \frac{1+\beta dc}{1-\beta dc\,[\Delta I_B / \Delta I_C]}$$

Substituting the value of $\Delta I_B / \Delta I_C$ in the above equation to get final expression for 'S'

- To obtain the value of 'S' $\Delta I_B / \Delta I_C$ apply KVL to input path :

$V_{CC} = R_C (I_C + I_B) + I_B R_B + V_{BE}$

$\therefore \quad V_{CC} = I_C R_C + I_B (R_B + R_C) + V_{BE}$ …(1)

To fine out stability factor 'S' we take into account the change is I_C due to change in I_{CBO}. The other two parameters V_{BE} & β_{dc} are assumed to be constant.

Change in I_C is ΔI_C, I_B is ΔI_B

$\therefore$ Equation (1) will be

$V_{CC} = \Delta I_C R_C + \Delta I_B (R_B + R_C) + V_{BE}$ …(2)

V_{CC} and V_{BE} are constant.

differentiate equation (2) w.r.t. ΔI_C we get,

$$0 = R_C + \frac{\Delta I_B}{\Delta I_C}(R_B + R_C) + 0$$

$$\frac{\Delta I_B}{\Delta I_C}(R_B + R_C) = - R_C$$

$$\frac{\Delta I_B}{\Delta I_C} = \frac{-R_C}{R_B + R_C} \quad \text{…(3)}$$

$$S = \frac{(1+\beta dc)}{1-\beta dc\left[\frac{-R_C}{R_B+R_C}\right]} = \frac{1+\beta dc}{1+\beta dc\left(\frac{R_C}{R_B+R_C}\right)}$$

As compared to fixed bias circuit collector to Base bias circuit has much lesser value of 'S'. This indicates that the Q pt stability is better for collector to Base bias circuit.

Q.4(a) Design a Mod 12 asynchronous counter using J–K Flipflop. **[10]**

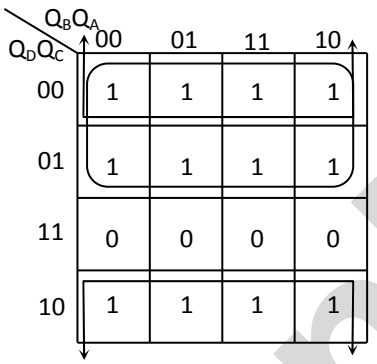
Ans.: Step 1: Since we have to design MOD–12counter, 4 flip flops are required.

Step 2: Truth table for the reset logic.

State	Flip Flop Outputs				Output of reset Logic 'y'	
	Q_D	Q_C	Q_B	Q_A		
0	0	0	0	0	1	
1	0	0	0	1	1	
2	0	0	1	0	1	
3	0	0	1	1	1	Valid State
4	0	1	0	0	1	
5	0	1	0	1	1	
6	0	1	1	0	1	
7	0	1	1	1	1	
8	1	0	0	0	1	
9	1	0	0	1	1	

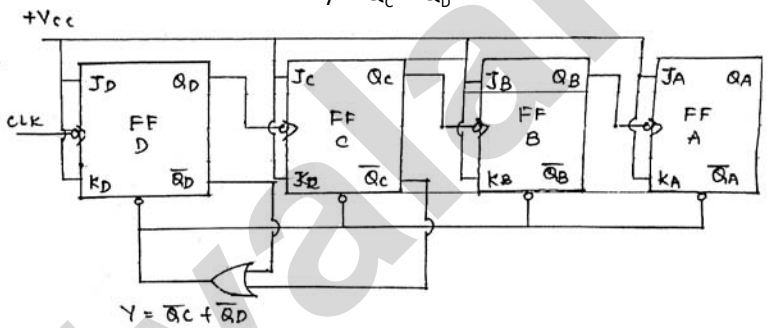
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

Step 3: K–map for 'y'



$y = \overline{Q}_C + \overline{Q}_D$

Step 4: Logic diagram



Q.4(b) Minimize the following four variable logic function using K-map [10]
f(A, B, C, D) = ∑m (0, 2, 3, 5, 6, 7, 8, 10, 11, 14, 15)
and design using only NAND gates.

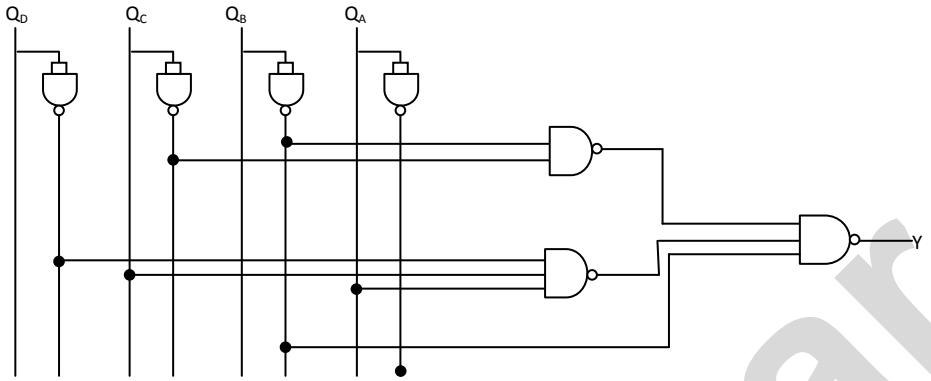
Ans.:

	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_D}\,\overline{Q_C}$	1	0	1	1
$\overline{Q_D}Q_C$	0	1	1	1
Q_DQ_C	0	0	1	1
$Q_D\overline{Q_C}$	1	0	1	1

$$Y = Q_B + \overline{Q_C}\,\overline{Q_A} + \overline{Q_D}\,Q_C\,Q_A$$

$$Y = \overline{\overline{Q_B + \overline{Q_C}\,\overline{Q_A} + \overline{Q_D}\,Q_C\,Q_A}}$$

$$= \overline{(\overline{Q_B}).(\overline{Q_C}Q_B).\overline{(\overline{Q_D}\,Q_C\,Q_A)}}$$



Q.5(a) Explain VHDL program format and write VHDL program for NAND gate. [10]

Ans.: VHDL program format :

VHDL is (VHSIC) HDL, i.e. very high speed Integrated circuit Hardware Description Language. If is a programming language for description the behavior of digital system.

VHDL is composed of all least three fundamental sections :

1) Library declaration : If contains a list of libraries to be used in the design. For example, ieee, std, work, etc.
2) Entity : Specifies the I/O pins of the circuit.
3) Architecture : Contains the VHDL code properties which describes how the circuit should behave.

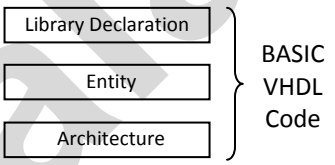


Fig. 1 : Fundamental units of VHDL code

1) Library Declaration :

- A Library is a collection of commonly used pieces of code.
- Placing such pieces inside a library allows them to be reused or shared by other destination.
- The code is usually written in the form of FUNCTIONS, PROCEDURE or COMPONENTS which are placed inside PACKAGES & then complied into the destination library.
- To declare a LIBRARY two Lines of code are needed, one containing name of the library & the other a use clause.

  For example : LIBRARY library–name;

  USE library–name––package–name. package–parts;
- At least three packages from three different libraries are usually needed in a design that are :

  ieee. std_logic_1164 (From the ieee library)

  Standard (from the std library)

  Work (work library)

- Declarations are as follows :

```
LIBRARY ieee;
USE ieee. std – logic – 1164.all;
LIBRARY std;
USE std. standard.all;
LIBRARY WORK;
USE Work.all;
```

2) Entity :

- A VHDL entity specifies the name of the entity, the ports of the entity & entity related information.
- All designs are created using one or more entities.
- Entity is the description of the interface between a design & external environment.
- An entity defines the input & output ports of a design.
- A design can contain more than one entity.
- Each entity has its own architecture statement.

Syntax : entity entity_name is
port(port_name : mode port_type;
port_name : mode port_type);
end entity_name;

Port–type : A previously defined data type.

Mode : There are five modes available in VHDL for ports (read value)/

1) In : Input port (read value)
2) Out : Output port
3) In out : bidirectional port
4) Buffer : Output port with read capability.

3) Architecture :

- It describes the underlying functionality or internal organization or operation of the entity & contains the statements that model the behavior of the entity.
- Architecture body is used to describe the behavior, data flow of structure of a design entity.
- Architecture body is use to describe internal details of a design entity using following modelling styles.
  1) Behaviour : As a set of sequential assignment statements.
  2) Data Flow : As a set of concurrent assignment statements.
  3) Structure : As a set of interconnected components.
  4) Mixed : As a set of combinational of above three.
- Architecture is always related to an entity & describes the behavior of that entity.

Syntax : Architecture architecture_name of entity_name is
{block_declarative_item}
begin
{concurrent_statement}
end [architecture_name];

VHDL program for NAND gate :

$y = \overline{AB}$

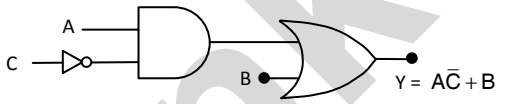
```
library IEEE;
Use IEEE. Std_logic_116 + .all,
entity UG is
port (A, B : in std_logic ;
          y : out std_logic );
end UG ;

architecture operation of UG is
begin
     y < = A NAND B;
end operation;
```

Q.5(b) Simplify following equation using Boolean algebra and Design using basic gates [10]
f(A, B, C) = A′B + BC′ + BC + AB′C′

Ans.: $f(A, B, C) = \overline{A}B + B\overline{C} + A\overline{B}\,\overline{C} + B\,C$

$$Y = \overline{A}B + B\overline{C} + A\overline{B}\,\overline{C} + B\,C$$
$$= \overline{A}B + \overline{C}(B + A\overline{B}) + B\,C$$
$$= \overline{A}B + \overline{C}(A + B) + B\,C$$
$$= \overline{A}B + A\overline{C} + B\overline{C} + BC$$
$$= \overline{A}B + A\overline{C} + B(\overline{C} + C)$$
$$= B(\overline{A} + 1) + A\overline{C}$$
$$Y = B + A\overline{C}$$



Q.6 Explain the following : [20]

Q.6(a) Explain 3-bit binary to Gray code conversion. [5]

Ans.: Step 1: i/p variables : B_2, B_1, B_0
o/p variables : G_2, G_1, G_0
$2^3 = 8$

Step 2: Truth Table

← i/p →			← o/p →		
B_2	B_1	B_0	G_2	G_1	G_O
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Step 3: K–map for G_2, G_1, G_0

1) k–map for G_2

B_2 \ B_1B_0	00	01	11	10
0	0	0	0	0
1	1	1	1	1

$G_2 = B_2$

2) k–map for G_1

B_2 \ B_1B_0	00	01	11	10
0	0	0	1	1
1	1	1	0	0

$G_1 = B_2 \overline{B}_1 + \overline{B}_2 B_1$

$G_1 = B_2 \oplus B_1$

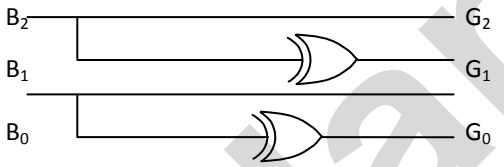
3) k–map for G_0

B_2 \ B_1B_0	00	01	11	10
0	0	1	0	1
1	0	1	0	1

$G_0 = \overline{B}_1 B_0 + B_1 \overline{B}_0$

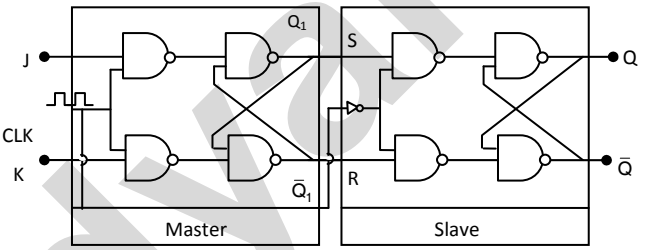
$G_0 = B_1 \oplus B_0$

Step 4: Logic diagram



Q.6(b) Explain working of Master slave J–K flip flop. **[5]**

Ans.:



- It is a combination of a clocked JK latch & clocked SR Latch.
- The clocked JK latch acts as the master & the clocked SR latch acts as the slave Master is positive level triggered. But due to the presence of the inverter in the clock line the slave will respond to the negative level.
- Hence, when Clock=1 the master is active & the slave is inactive, whereas when clock=0 the slave is active & the master is inactive.

Working :

Case 1: Clock = X, J = K = 0 & Clock = 1, J = K = 0

- For CLK = 1 the master is active, slave is inactive., As J = K = 0, Q_1 & Q_2 will not change.
- Hence S & R inputs to the slave will retain unchanged.
- As soon as CLK = 0, the slave become active & Master inactive. But since the S & R inputs have not changed, the salve outputs will also remain unchanged.

  ∴ The output will not change if J = K = 0

Case 2: Clock = ⎍, J = 0, K = 1

- CLK = 1, Master is active & slave is inactive
  ∴ outputs of the master become $Q_1 = 0$ & $\overline{Q}_1 = 1$. That means S = 0 & R = 1, Clock = 0; Slave is active & Master inactive output of the slave become Q = 0 & $\overline{Q}_1 = 1$.
- Again of CLK = 1, M = active, S = inactive, even if the changed outputs Q = 0 & $\overline{Q}_1 = 1$, fed back to master, its outputs will be $Q_1 = 0$ & $\overline{Q}_1 = 1$.
  That means S = 0 & R = 1.
  Hence with CLK = 0 & 'S' becoming active the outputs of slave will remain Q = 0 & $\overline{Q}_1 = 1$.

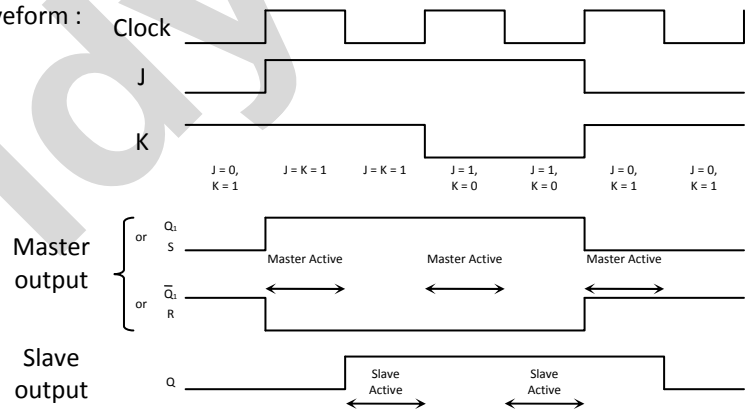
Case 3: CLK = ⎍, J = 1, K = 0

- CLK = 1, M = active & S = inactive
  ∴ Outputs of master become $Q_1 = 1$ & $\overline{Q}_1 = 0$, i.e. S = 1 & R = 0
- CLK = 0, M = inactive & S = active
  ∴ Outputs of slave become Q = 1 & $\overline{Q} = 0$
- Again if clock = 1 then it can be shown that the outputs of the slave are stabilized to Q = 1 & $\overline{Q} = 0$.

Case 4: CLK = ⎍ , J = K, K = 1

- CLK = 1, M = active & S = inactive
  Outputs of Master will toggle. So S & R also will be inverted.
- CLK = 0, M = inactive & S = active
  ∴ Outputs of Slave will toggle.
  These changed outputs are returned back to the Master inputs.
  But since CLK = 0, the master is still inactive so it does not respond to these changed.
- This avoids the multiple toggling which leads to the race around condition.
- Thus the Master slave Flip flip will avoid the race around condition.

Waveform :



Q.6(c) Explain working Current Mirror Circuit. **[5]**

Ans.:

- The circuit in which the output current is forced to be equal to the input current is called as current mirror circuit.

- In other words in a current mirror circuit, the output current is the mirror image of input current.

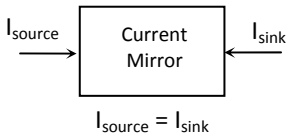


Fig.1 : Block Diagram

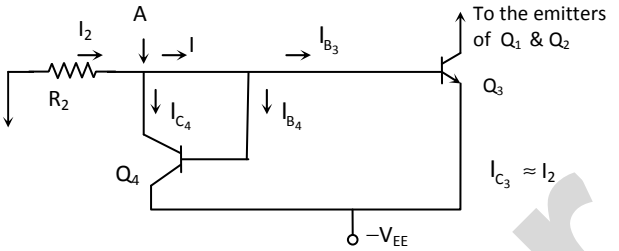


Fig.2 : Circuit Diagram

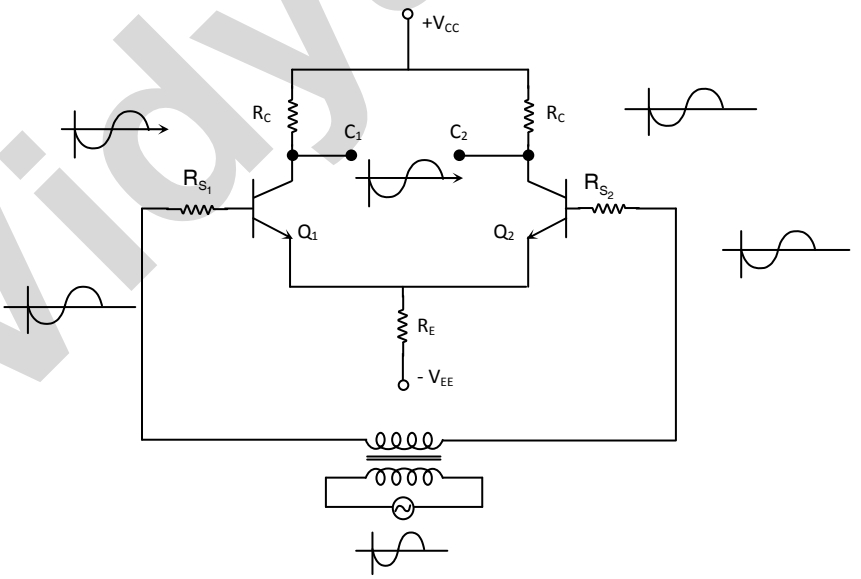
Operation :

- The current mirror is a special case of constant current bias & hence it can be used to provide a constant current for the two transistors Q_1 & Q_2 in the differential AMP circuit.
- The transistors Q_3 & Q_4 are identical transistors with equal currents & voltages.
  $\therefore \quad V_{BE3} = V_{BE4}, \; I_{C3} = I_{C4}$ & $I_{B3} = I_{B4}$
- Apply KCL at node 'A'
  $I_2 = I_{C4} + I = I_{C4} + I_{B3} + I_{B4} = I_{C4} + 2I_{B4}$
  $\therefore \quad I_{B3} = I_{B4}$
  Also $I_2 = I_{C3} + 2I_{B3}$ $\quad \because \quad I_{C3} = I_{C4}$ & $I_{B3} = I_{B4}$
  $$\therefore \quad I_2 = I_{C3} + 2\,\frac{I_{C3}}{\beta_{dc}} = I_{C3}\left(1 + \frac{2}{\beta_{dc}}\right)$$
- As β_{dc} is large, the second term can neglected.
  $I_2 \approx I_{C3}$

Q.6(d) Explain working of Differential Amplifier. [5]

Ans.:

- Differential Amplifier is a device which amplifies differential between two signal
  $V_0 < (V_1 - V_2)$
- Operation of the Basic differential Amplifier in differential mode –



- For operation in the differential modes we need to have the two i/p signal V_{s1} and V_{s2} of equal magnitude but opposite phase.
- i.e. $V_{s1} = -V_{s2}$ & their magnitude should be equal. In order to get there signal a centre tapped X^{mas} is oved.
- In positive half cycle of 'V_s' the input to Q_1 is the Sinusoidal signal and the output to Q_2 is –Ve Sinusoidal signal.
  This is due to centre tapped X^{men}
- Output is equal to differential between output of individual transistors.
- It's amplitude will be twice the amplitude of the signal Voltage obtained either collector to ground.
- The output voltage waveform shown in fig is the w/f at collector of Q_1 wrt collector of Q_2.
- In the +Ve half cycle of source at input of Q_1 is +Ve. Hence +Ve voltage is developed a cross R_E. This is became Q_1 acts as the Emitter follower.
- At the same time Q_2 receiver a –Ve voltage at it's input & hence produces –Ve voltage across R_E due to Emitter follower action.
- Thus equal & opposite signal voltage appear across R_E & cancel each other.
  Therefore when we consider the effect of Q_1 and Q_2. Simultaneously, no signal voltage appears acorss R_E & the signal current flowing through R_E is equal to Zero .
  Therefore R_E does not introduce –Ve F/B thus is the differential mode, the signal applied to the Bases of the two transistors are equal to magnitude but opposite is sign.

❑❑❑❑❑