UNIVERSITY OF MUMBAI

Bachelor of Electronics Engineering

Third Year (Semester VI), Revised course

(Rev2012) From Academic Year 2014-15

(As per Credit Based Semester and Grading System with effect from the academic year 2012–2013)

Semester VI

Sub Code	Subject Title	Teaching Scheme (Hrs.)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC601	Basic VLSI Design	04	--		04	--		04
EXC602	Advanced Instrumentation Systems	04	--	--	04	--	--	04
EXC603	Computer Organization	04	--	--	04	--	--	04
EXC604	Power Electronics I	04	--	--	04	--	--	04
EXC605	Digital Signal Processing and Processors	04	--	--	04	--	--	04
EXC606	Modern Information Technology for Management	02	--	--	02	--	--	02
EXL601	VLSI Design Laboratory	--	02	--	--	01	--	01
EXL602	Advance Instrumentation and Power Electronics Laboratory	--	02	--	--	01	--	01
EXL605	Digital Signal Processing and Processors Laboratory	--	02	--	--	--	--	--
EXL603	Mini Project II	--	#02	--	--	02	--	02
Total		**22**	**08**	--	**22**	**04**	--	**26**

 # Class wise

Semester VI

Subject Code	Subject Title	Examination Scheme							
		Theory Marks				Term Work	Practical and Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. of Test 1 & Test 2					
EX601	Basic VLSI Design	20	20	20	80	--	--	--	100
EX602	Advanced Instrumentation Systems	20	20	20	80	--	--	--	100
EX603	Computer Organization	20	20	20	80	--	--	--	100
EX604	Power Electronics I	20	20	20	80	--	--	--	100
EX605	Digital Signal Processing and Processors	20	20	20	80	--	--	--	100
EXC606	Modern Information Technology for Management	10	10	10	40	--	--	--	50
EXL601	VLSI Design Laboratory	--	--	--	--	25	--	25	50
EXL602	Advance Instrumentation and Power Electronics Laboratory	--	--	--	--	25	--	25	50
EXL605	Digital Signal Processing and Processors Laboratory	--	--	--	--	25	25	--	50
EXL603	Mini Project II	--	--	--	--	25	25	--	50
Total		**110**	**110**	**110**	**440**	**100**	**50**	**50**	**750**

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC601	Basic VLSI Design	04	--	--	04	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXC601	Basic VLSI Design	20	20	20	80	--	--	--	100

Course Pre-requisite:

- EXC302: Electronic Devices
- EXC303: Digital Circuits and Design
- EXC402: Discrete Electronic Circuits
- EXC502: Design With Linear Integrated Circuits

Course Objectives:

1. To teach fundamental principles of VLSI circuit design and layout techniques
2. To highlight the circuit design issues in the context of VLSI technology

Course Outcomes:

After successful completion of the course student will be able to

1. demonstrate a clear understanding of choice of technology and technology scaling
2. design MOS based circuits and draw layout
3. realize logic circuits with different design styles
4. demonstrate a clear understanding of system level design issues such as protection, timing and power dissipation

Module No.	Unit No.	Topics	Hrs.
1		**Technology Trend**	6
	1.1	**Technology Comparison:** Comparison of BJT, NMOS and CMOS technology	
	1.2	**MOSFET Scaling:** Types of scaling, Level 1 and Level 2 MOSFET Models, MOSFET capacitances	
2		**MOSFET Inverters**	10
	2.1	**Circuit Analysis:** Static and dynamic analysis (Noise, propagation delay and power dissipation) of resistive load and CMOS inverter, comparison of all types of MOS inverters, design of CMOS inverters, CMOS Latch-up	
	2.2	**Logic Circuit Design:** Analysis and design of 2-I/P NAND and NOR using equivalent CMOS inverter	

3		**MOS Circuit Design Styles**	**10**
	3.1	**Design Styles:** Static CMOS, pass transistor logic, transmission gate, Pseudo NMOS, Domino, NORA, Zipper, C^2MOS, sizing using logical effort	
	3.2	**Circuit Realization:** SR Latch, JK FF, D FF, 1 Bit Shift Register, MUX, decoder using above design styles	
4		**Semiconductor Memories**	**08**
	4.1	**SRAM:** ROM Array, SRAM (operation, design strategy, leakage currents, read/write circuits), DRAM (Operation 3T, 1T, operation modes, leakage currents, refresh operation, Input-Output circuits), Flash (mechanism, NOR flash, NAND flash)	
	4.2	**Peripheral Circuits:** Sense amplifier, decoder	
5		**Data Path Design**	**08**
	5.1	**Adder:** Bit adder circuits, ripple carry adder, CLA adder	
	5.2	**Multipliers and shifter:** Partial-product generation, partial-product accumulation, final addition, barrel shifter	
6		**VLSI Clocking and System Design**	**10**
	6.1	**Clocking:** CMOS clocking styles, Clock generation, stabilization and distribution	
	6.2	**Low Power CMOS Circuits:** Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling	
	6.3	**IO pads and Power Distribution:** ESD protection, input circuits, output circuits, simultaneous switching noise, power distribution scheme	
	6.4	**Interconnect:** Interconnect delay model, interconnect scaling and crosstalk	
		Total	**52**

Recommended Books:

1. Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.
3. Etienne Sicard and Sonia Delmas Bendhia, "*Basics of CMOS Cell Design*", Tata McGraw Hill, First Edition.
4. Neil H. E. Weste, David Harris and Ayan Banerjee, "*CMOS VLSI Design: A Circuits and Systems Perspective*", Pearson Education, 3rd Edition.
5. Debaprasad Das, "*VLSI Design*", Oxford, 1st Edition.
6. Kaushik Roy and Sharat C. Prasad, "*Low-Power CMOS VLSI Circuit Design*", Wiley, Student Edition.

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC602	Advanced Instrumentation System	04	--	--	04	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
EXC602	Advanced Instrumentation System	20	20	20	80	--	--	--	100

Course Objectives:

1. To understand basic functions and working of Pneumatic and Hydraulic components used in Instrumentation Process System.
2. To understand principles of process parameter transmission and conversion of process parameters to electrical and vice versa.
3. To become familiar with control system components and their application in process control.
4. Learners are expected to understand various controllers used in process control and the tuning methods of controllers.

Module No.	Unit No.	Topics	Hrs.
1.	1.1	**Concepts of Advancement in Instrumentation**	06
		Data acquisition and data logging, telemetry in measurement, basic requirement of control system and components	
2		**Pneumatic Components**	12
	2.1	ISO symbols, pneumatic air supply system, air compressors, pressure regulation devices, directional control valves	
	2.2	**Special types of pneumatic valve:** pilot-operated valves, non-return valves, flow control valves, sequence valves, and time delay valve	
	2.3	Single and double acting linear actuators, special type of double acting cylinder, rotary actuators, air motors	
	2.4	**Process control pneumatics:** flapper nozzle system, volume boosters, air relays, pneumatic transmitters and controllers, pneumatic logic gates, dynamic modeling of pneumatic circuits	
3		**Hydraulic Components**.	06
	3.1	Hydraulic pumps, Pressure regulation method, loading valves	
	3.2	Hydraulic valves and actuators, speed control circuits for hydraulic actuators	
	3.3	Selection and comparison of pneumatic, hydraulic and electric systems	

4		**Transmitters and Converters**	**12**
	4.1	Electronic versus pneumatic transmitters, 2-wire; 3-wire and 4-wire current transmitters	
	4.2	**Electronic type:** temperature, pressure, differential pressure, level, flow transmitters and their applications Smart (Intelligent) transmitters, Buoyancy transmitters and their applications.	
	4.3	**Converters**: Pneumatic to Electrical and Electrical to Pneumatic converters	
5		**Process Control Valves**	**08**
	5.1	Globe, ball, needle, butterfly, diaphragm, pinch, gate, solenoid, smart control valves and special designs of globe valves	
	5.2	Flow characteristics, control valve parameters, control valve capacity, valve rangeabilty, turn-down, valve size, valve gain	
	5.3	Selection criteria, specifications and installation of control valves	
	5.4	**Valve Positioners**: Necessity, types-motion balance and force-balance, effect on performance of control valve	
	5.5	**Control Valve Actuators:** Electrical, pneumatic, hydraulic, electro-mechanical, digital actuators. selection criteria of valve actuators	
6		**Controllers and Controller Tuning**	**08**
	6.1	**Continuous and discontinuous controller:** proportional controller, proportional band, RESET controller, rate controller, composite controller, cascade controller, feed-forward controller	
	6.2	Need and different method of controller tuning	
		Total	**52**

Recommended Books:

1. Bella G. Liptak, "*Process Control and Optimization, Instrument Engineer's Handbook"*, 4th Edition, CRC Press
2. WG Andrews and Williams, "*Applied Instrumentation in the process Industries, Vol. - I and II*", Gulf Publication
3. Terry Barlett, "*Process Control System and Instrumentation*", Delimar Cengage learning Reprint-2008
4. Andrew Parr, "*Hydraulics And Pneumatics- A Technician's And Engineer's Guide*", Jaico Publishing House, Mumbai
5. C.D.Johnson, "*Process Control and Instrument Technology"*, Tata Mcgraw Hill.
6. J. W. Hatchison, "*ISA Handbook of Control Valves*", 2nd Edition, ISA, 1990.

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC603	Computer Organization	04	--	--	04	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXC603	Computer Organization	20	20	20	80	--	--	--	100

Course objectives:

1. To conceptualize the basics of organizational and architectural issues of a digital computer.
2. To analyze performance issues in processor and memory design of a digital computer.
3. To understand various data transfer techniques in digital computer.
4. To analyze processor performance improvement using instruction level parallelism.

Course Outcomes:

The student should be able:

1. To understand basic structure of computer.
2. To perform computer arithmetic operations.
3. To understand control unit operations.
4. To understand the concept of cache mapping techniques.
6. To design memory organization (banks for different word size operations).
5. To understand the concept of I/O organization.
6. To conceptualize instruction level parallelism.

Module No.	Unit No.	Topics	Hrs.
1		Introduction to Computer Organization	10
	1.1	Fundamental units of computer organization, evolution of computers, von neumann model, performance measure of computer architecture	
	1.2	Introduction to buses and connecting I/O devices to CPU and Memory, bus structure,	
	1.3	Introduction to number representation methods, integer data computation, floating point arithmetic.	
2		Processor Organization and Architecture	14
	2.1	CPU Architecture, register organization, instruction formats, basic instruction cycle, instruction interpretation and sequencing	
	2.2	**Control unit:** soft wired (micro-programmed) and hardwired control unit design methods	
	2.3	Microinstruction sequencing and execution, micro operations, concepts of nano programming.	
	2.4	Introduction to RISC and CISC architectures and design issues, case study on 8085 microprocessor, features, architecture, pin configuration and addressing modes	

3		**Memory Organization**	**12**
	3.1	Introduction to memory and memory parameters, classifications of primary and secondary memories, types of RAM and ROM, allocation policies, memory hierarchy and characteristics	
	3.2	Cache memory concept, architecture (L1, L2, L3), mapping techniques, cache coherency	
	3.3	Interleaved and associative memory, virtual memory, concept, segmentation and paging, page replacement policies	
4		**Input / Output Organization**	**8**
	4.1	Types of I/O devices and access methods, types of buses and bus arbitration, I/O interface, serial and parallel ports	
	4.2	Types of data transfer techniques, programmed I/O, interrupt driven I/O and DMA	
	4.3	Introduction to peripheral devices, scanner, plotter, joysticks, touch pad, storage devices	
5		**Introduction To Parallel Processing System**	**4**
	5.1	Introduction to parallel processing concepts, Flynn's classifications, pipeline processing, instruction pipelining, pipeline stages, pipeline hazards	
6		**Introduction to Intel IA32 Architecture**.	**4**
	6.1	Intel IA32 family architecture, register structure, addressing modes, advancements in arithmetic and logical instructions, exception handling in IA32 architecture	
		Total	**52**

Recommended Books:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "*Computer Organization*", Fifth Edition, Tata McGraw-Hill.
2. John P. Hayes, "*Computer Architecture and Organization*", Third Edition.
3. William Stallings, "*Computer Organization and Architecture: Designing for Performance*", Eighth Edition, Pearson.
4. B. Govindarajulu, "*Computer Architecture and Organization: Design Principles and Applications*", Second Edition, Tata McGraw-Hill.
1. Dr. M. Usha and T. S. Srikanth, "*Computer System Architecture and Organization*", First Edition, Wiley-India.
2. Ramesh Gaonkar, "*Microprocessor Architecture, Programming and Applications with the 8085"*, Fifth Edition,Penram.

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC604	Power Electronics I	04	--	--	04	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXC604	Power Electronics I	20	20	20	80	--	--	--	100

Course Pre-requisite:

- EXC302: Electronic Devices

Course Objectives:

1. To teach power electronic devices and there characteristics.
2. To highlight power electronic based rectifier, inverter and chopper.

Course Outcomes:

After successful completion of the course student will be able to

1. Discuss tradeoffs involved in power semiconductor devices.
2. Analyze different types of rectifier and inverter.
3. Carry out verifications of issues involved in rectifier via simulations

Module No.	Unit No.	Contents	Hrs.
1		**Silicon Controlled Rectifiers**	10
	1.1	Principle of operation of SCR, static and dynamic characteristics, gate characteristics	
	1.2	Methods of turning on (type of gate signal), firing circuits (using R, R-C, UJT),commutation circuit	
	1.3	Protection of SCR	
2		**Other Switching Devices**	08
	2.1	**Principle of operation, characteristics, rating and applications of:** TRIAC, DIAC, GTO, MOSFET, IGBT and power BJT	
	2.2	Driver circuits for power transistors	
3		***Controlled Rectifiers**	12
	3.1	Half wave controlled rectifiers with R, R-L load,	
	3.2	Full wave controlled rectifiers, half controlled and fully controlled rectifiers with R, R-L load **(effect of source inductance not to be considered)**	
	3.3	Single phase dual converter, three phase half controlled and fully controlled rectifiers with R load only ***Numerical based on calculation of output voltage**	

4		***Inverters**	**10**
	4.1	**Introduction, principle of operation, performance parameters of:** Single phase half / full bridge voltage source inverters with R and R-L load, three phase bridge inverters (120^0 and 180^0 conduction mode) with R and R-L load	
	4.2	Voltage control of single phase inverters using PWM techniques, harmonic neutralization of inverters, applications ***Numerical with R load only**	
5		**Choppers**	**6**
	5.1	Basic principle of step up and step down choppers	
	5.2	**DC-DC switching mode regulators:** Buck, Boost, Buck-Boost, Cuk regulators, (CCM mode only)	
6		**AC Voltage Controllers**	**4**
	6.1	Principle of On-Off control, principle of phase control, single phase bidirectional control with R and RL load	
7		**Cycloconvertor**	**2**
	7.1	Introduction, single phase and three phase Cyclo-converters, applications	
		Total	**52**

Recommended Books:

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1. M. H. Rashid, "*Power Electronics*", Prentice-Hall of India
2. Ned Mohan, "*Power Electronics*", Undeland, Robbins, John Wiley Publication
3. Ramamurthy, " *Thyristors and Their Applications*"
4. Alok Jain, "*Power Electronics and its Applications*", Penram International Publishing (India) Pvt. Ltd.
5. Vedam Subramanyam, "*Power Electronics*", New Age International
6. Landers, "*Power Electronics*", McGraw Hill
7. M.D. Singh and K. B. Khanchandani, "*Power Electronics*", Tata McGraw Hill
8. P. C. Sen, "*Modern Power Electronics*", Wheeler Publication

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

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Subject Code	Subject Name	Teaching Scheme (Hrs.)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC 605	Digital Signal Processing and Processors	4	--	--	4	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
EXC 605	Digital Signal Processing and Processors	20	20	20	80	--	--	--	100

Course Objective:

1. To study DFT and its computation
2. To study the design techniques for digital filters
3. To study the finite word length effects in signal processing
4. To study the fundamentals of digital signal processors
5. To get acquainted with the DSP applications

Course Outcome:

Students will be able to understand concept of digital filters

1. Students will be able to decide the selection and design of digital filters
2. Students will understand the effect of hardware limitation
3. Students will be understand need of DSP processors
4. Students will be able to understand the use and application of DSP processors

Module No.	Unit No.	Topics	Hrs.
1.0		Discrete Fourier Transform and Fast Fourier Transform	10
	1.1	**Discrete Fourier Series**: Properties of discrete Fourier series, DFS representation of periodic sequences.	
	1.2	**Discrete Fourier transforms**: Properties of DFT, linear convolution of sequences using DFT, computation of DFT, relation between Z-transform and DFS	
	1.3	**Fast Fourier Transforms**: Fast Fourier transforms (FFT), Radix-2 decimation in time and decimation in frequency FFT algorithms, inverse FFT, and composite FFT	
2.0		IIR Digital Filters	10
	2.1	Mapping of S-plane to Z-plane, impulse invariance method, bilinear Z transformation (BLT) method, frequency warping, pre-warping	
	2.2	**Analog filter approximations**: Butter worth and Chebyshev, design of IIR digital filters from analog filters, design examples	
	2.3	Analog and digital frequency transformations	
3.0		FIR Digital Filters	10
	3.1	Characteristics of FIR digital filters, frequency response, location of the zeros of linear phase FIR filters	

	3.2	Design of FIR digital filters using window techniques, Gibbs phenomenon, frequency sampling technique, comparison of IIR and FIR filters	
4.0		**Finite Word Length Effects in Digital Filters**	**08**
	4.1	Number representation, fixed point, sign-magnitude, one's complement, two's complement forms, floating point numbers	
	4.2	Quantization, truncation, rounding, effects due to truncation and rounding, Input quantization error, Product quantization error, co-efficient quantization error, zero-input limit cycle oscillations, overflow limit cycle oscillations, scaling	
	4.3	Quantization in Floating Point realization IIR digital filters, finite word length effects in FIR digital filters, quantization effects in the computation of the DFT- quantization errors in FFT algorithms	
5.0		**Introduction to DSP Processors**	**08**
	5.1	Introduction to fixed point and floating point DSP processor, multiplier and multiplier accumulator (MAC), modified bus structures and memory access schemes in DSPs, multiple access memory, multiport memory, VLIW architecture, pipelining, special addressing modes, on-chip peripherals	
	5.2	Features of TMS 320c67xx DSP processor, architecture of TMS 320c67xx DSP processor, architecture features: computational units, bus architecture memory, data addressing, address generation unit, program control, program sequencer, pipelining, interrupts, features of external interfacing, on-chip peripherals, hardware timers, host interface port, clock generators, SPORT	
6.0		**Applications of DSP Processors**	**06**
	6.1	Speech Processing: Speech analysis, speech coding, sub band coding, channel vocoder, homomorphic vocoder, digital processing of audio signals.	
	6.2	**Radar signal processing**: Radar principles, radar system and parameter considerations, signal design	
Total			**52**

Recommended Books:

1. Proakis J., Manolakis D., "*Digital Signal Processing*", 4th Edition, Pearson Education
2. Oppenheim A., Schafer R., Buck J., "*Discrete Time Signal Processing*", 2nd Edition, Pearson Education.
3. Babu R., "*Digital Signal Processing*", 4th Edition, Scitech Publications.
4. B. Venkata Ramani and M. Bhaskar, "*Digital Signal Processors, Architecture, Programming and Applications*", Tata McGraw Hill, 2004.
5. L. R. Rabiner and B. Gold, "*Theory and Applications of Digital Signal Processi*ng", Prentice-Hall of India, 2006.
6. B. Kumar, "*Digital Signal Processing*", New Age International Publishers, 2014.

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

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Subject Code	Subject Name	Teaching Scheme (Hrs.)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC 606	Information Technology For Management of Enterprises	2	--	--	2	--	--	02

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
EXC 606	Information Technology For Management of Enterprises	10	10	10	40	--	--	--	50

Course Objectives:

1. The course contains the basics of Information Technology and its application in a business environment.
2. To know about E- Business using Information systems with the help of case studies, exhibits, diagrams and illustrations.

Course outcomes:

1. Student will explore production tools, various protocols which run the business infrastructure system and business system managements
2. Students will learn importance of IT tools in content management
3. Student will learn Management Information System and its application in various businesses.

Module No.	Unit No.	Topics	Hrs.
1		IT Infrastructure	6
	1.1	Information technology	
	1.2	Computing infrastructure: software	
	1.3	Networking infrastructure	
	1.4	Cabling infrastructure	
	1.5	Wires less infrastructure	
	1.6	Storage infrastructure	
2		IT Production Tool	6
	2.1	Security infrastructure	
	2.2	Office tools	
	2.3	Data management tools	
	2.4	Web tools	
3		Internet and Network Protocol	4
	3.1	Network management tools	
	3.2	Network protocols and global connectivity	

4		**IT Management**	**6**
	4.3	E-Business Highway- Business Automation Platform	
	4.4	Infrastructure Management	
	4.5	Security Management	
	4.6	Information Management and Audit	
5		**IT Applications**	**4**
	5.1	E Governance	
	5.2	Connected world and E-commerce	
	5.3	Information Systems	
	5.4	Business Systems	
		Total	**26**

Reference Books:

1. B Muthukumaran, "*Information Technology for Management*", Oxford University Press
2. Kenneth C. Laudon and Jane P. Laudon, "*Management Information Systems*", Pearson Education

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each carrying 10 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXL601	Basic VLSI Design Laboratory	--	02	--	--	01	--	01

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical and Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXL601	Basic VLSI Design Laboratory	--	--	--	--	25	--	25	50

Term Work:
At least 10 experiments based on the entire syllabus of Subject **EXC601 (VLSI Design)** should be set to have well predefined inference and conclusion. Computation/simulation based experiments are encouraged. The experiments should be students' centric and attempt should be made to make experiments more meaningful, interesting and innovative. Term work assessment must be based on the **overall performance** of the student with **every experiment graded from time to time**. The grades should be converted into marks as per the **Credit and Grading System** manual and should be **added and averaged**. The grading and term work assessment should be done based on this scheme.
The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
Oral exam will be based on the entire syllabus

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXL605	Digital Signal Processing and Processors Laboratory	--	02	--	--	01	--	01

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical and Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXL605	Digital Signal Processing and Processors Laboratory	--	--	--	--	25	--	25	50

Term Work:

At least 10 experiments based on the entire syllabus of Subject **EXC605 Digital Signal Processing and Processors** should be set to have well predefined inference and conclusion. Computation/simulation based experiments are encouraged. The experiments should be students' centric and attempt should be made to make experiments more meaningful, interesting and innovative. Term work assessment must be based on the **overall performance** of the student with **every experiment graded from time to time**. The grades should be converted into marks as per the **Credit and Grading System** manual and should be **added and averaged**. The grading and term work assessment should be done based on this scheme.

The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.

Oral exam will be based on the entire syllabus

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXL602	Advanced Instrumentation and Power Electronics Laboratory	--	02	--	--	01	--	01

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical and Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXL602	Advanced Instrumentation and Power Electronics Laboratory	--	--	--	--	25	25	--	50

Term Work:

At least 10 experiments based on the entire syllabus of Subject **EXC602 and EXC 604** should be set to have well predefined inference and conclusion. Computation/simulation based experiments are encouraged. The experiments should be students' centric and attempt should be made to make experiments more meaningful, interesting and innovative. Term work assessment must be based on the **overall performance** of the student with **every experiment graded from time to time**. The grades should be converted into marks as per the **Credit and Grading System** manual and should be **added and averaged**. The grading and term work assessment should be done based on this scheme.

The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.

Practical and oral exam will be based on the entire syllabus of **EXC602 and EXC 604**

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETL603	Mini Project II	--	02	--	--	01	--	01

Course Code	Course Name	Examination Scheme						
		Theory Marks				Term Work	Practical/ Oral	Total
		Internal assessment			End Sem. Exam			
		Test 1	Test 2	Ave. Of Test 1 and Test 2				
ETL603	Mini Project II	--	--	--	--	25	25	50

Term Work:

The main intention of Mini Project is to make student enable to apply the knowledge and skills learned out of courses studied to solve/implement predefined practical problem. The students undergo various laboratory/tutorial/simulation laboratory/work shop courses in which they do experimentation based on the curriculum requirement. The mini Project may be beyond the scope of curriculum of courses taken or may be based on the courses but thrust should be on

- Learning additional skills
- Development of ability to define and design the problem and lead to its accomplishment with proper planning.
- Learn the behavioral science by working in a group

The group may be maximum **four** (04) students. Each group will be assigned one faculty as a supervisor. The college should keep proper assessment record of progress of the project and at the end of the semester it should be assessed for awarding TW marks. The TW may be examined by approved internal faculty appointed by the head of the institute. The final examination will be based on demonstration in front of internal and external examiner. In the examination each individual student should be assessed for his/her contribution, understanding and knowledge gained about the task completed.

The topic of Mini Project I and II may be different and / or may be advancement in the same topic. The students may use this opportunity to learn different computational techniques as well as some model development. This they can achieve by making proper selection of Mini Projects.