UNIVERSITY OF MUMBAI

Bachelor of Engineering
Electronics and Telecommunication Engineering

Third Year Engineering

(Sem. Sem. VI), (Rev-2012)

effective from Academic Year 2014 -15

Under

FACULTY OF TECHNOLOGY

(As per Semester Based Credit and Grading System)

SEMESTER VI

Course Code	Course Name	Teaching Scheme (Hrs.)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ETC601	Digital Communication	04	--		04	--		04
ETC602	Discrete Time Signal Processing	04	--	--	04	--	--	04
ETC603	Computer Communication and Telecom Networks	04	--	--	04	--	--	04
ETC604	Television Engineering	04	--	--	04	--	--	04
ETC605	Operating Systems	04	--	--	04	--	--	04
ETC606	VLSI Design	04	--	--	04	--	--	04
ETL601	Discrete Time Signal Processing Laboratory	--	02	--	--	01	--	01
ETL602	Communication Engineering Laboratory III		02			01	--	01
ETL603	Communication Engineering Laboratory IV	--	02	--	--	01	--	01
ETL604	Mini Project II	--	02	--	--	01	--	01
Total		**24**	**08**	**--**	**24**	**04**	**--**	**28**

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical And Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. of Test 1 & Test 2					
ETC601	Digital Communication	20	20	20	80	--	--	--	100
ETC602	Discrete Time Signal Processing	20	20	20	80	--	--	--	100
ETC603	Computer Communication and Telecom Networks	20	20	20	80	--	--	--	100
ETC604	Television Engineering	20	20	20	80	--	--	--	100
ETC605	Operating Systems	20	20	20	80	--	--	--	100
ETC606	VLSI Design	20	20	20	80	--	--	--	100
ETL601	Discrete Time Signal Processing Laboratory	--	--	--	--	25	25	--	50
ETL602	Communication Engineering Laboratory III	--	--	--	--	25	25	--	50
ETL603	Communication Engineering Laboratory IV	--	--	--	--	25	25	--	50
ETL604	Mini Project II	--	--	--	--	25	25	--	50
Total		**120**	**120**	**120**	**480**	**100**	**100**	**--**	**800**

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETC601	Digital Communication	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETC601	Digital Communication	20	20	20	80	-	-	-	100

Pre-requisite:

- ETC405 Signal and System,
- ETC502 Analog Communication,
- ETC503 Random Signal Analysis

Course Objective:

- Aim is to identify the functions of different components
- Learn about theoretical bounds on the rates of digital communication system and represent a digital signal using several modulation methods
- Draw signal space diagrams, compute spectra of modulated signals and apply redundancy for reliable communication.

Course Outcome: At the end of course, student will be able to :

- Understand the basics of information theory and coding techniques.
- Determine the minimum number of bits per symbol required to represent the source and the maximum rate at which a reliable communication can take place over the channel.
- Describe and determine the performance of different waveform techniques for the generation of digital representation of signals.
- Determine methods to mitigate inter symbol interference in baseband transmission system.
- Describe and determine the performance of different error control coding schemes for the reliable transmission of digital representation of signals and information over the channel.
- Understand various spreading techniques and determine bit error performance of various digital communication systems.

Module No.		Topics	Hrs.
1.		**Information theory and source coding**	6
	1.1	Block diagram and sub-system description of a digital communication system, measure of information and properties, entropy and it's properties	
	1.2	Source Coding, Shannon's Source Coding Theorem, Shannon-Fano Source Coding, Huffman Source Coding	
	1.3	Differential Entropy, joint and conditional entropy, mutual information and channel capacity, channel coding theorem, channel capacity theorem	
2		**Baseband Modulation and Transmission**	6
	2.1	Discrete PAM signals and it's power spectra	
	2.2	Inter-symbol interference, Nyquist criterion for zero ISI, sinusoidal roll-off filtering, correlative coding, equalizers, and eye pattern	
3		**Base band Detection**	5
	3.1	Orthogonality, representation of signals	
	3.2	Maximum likelihood decoding	
	3.3	Correlation receiver, equivalence with matched filter	
4		**Bandpass Modulation and Demodulation**	12
	4.1	Bandpass digital transmitter and receiver model, digital modulation schemes	
	4.2	**Generation, detection, signal space diagram, spectrum, bandwidth efficiency, and probability of error analysis of:** Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK)Modulations, Binary Phase Shift Keying (BPSK) Modulation, Quaternary Phase Shift Keying QPSK), M-ary PSK Modulations, Quadrature Amplitude Modulation (QAM), Minimum Shift Keying (MSK)	
	4.3	Comparison between bandwidth and bit rate, applications of digital modulation schemes	
5		**Error Control Systems**	10
	5.1	Types of error control, error control codes, linear block codes, vector spaces ,vector sub spaces, generator matrix, systematic linear block codes, parity check matrix, syndrome testing ,error correction, and decoder implementation	
	5.2	**Cyclic codes:** Algebraic structure of cyclic codes, binary cyclic code properties, encoding in systematic form, circuits for dividing polynomials, systematic encoding with shift register and error detection	
	5.3	**Convolution Codes:** Time domain and transform domain approach, graphical representation, code tree, trellis, state diagram, decoding methods, maximum likelihood decoding, and free distance	7
	5.4	Viterbi decoding, hard decision Viterbi decoding , decoding window, soft decision Viterbi decoding, code spectra, recursive systematic codes, code transfer function, and application areas	
6		**Spread Spectrum**	6
	6.1	Spread Spectrum (SS) concept, PN Sequences, Direct Sequence(DS), Frequency Hopping (FH), and Time Hopping	
	6.2	Comparison of Spread Spectrum Methods, SS Communication System, DSSS with Coherent BPSK, Processing Gain, Probability of Error of FHSS Transmitter and FHSS Receiver	
Total			**52**

Recommended Books:

1. Sklar B, and Ray P. K., *"Digital Communication: Fundamentals and applications,"* Pearson, Dorling Kindersley (India), Delhi, Second Edition, 2009.
2. Haykin Simon, *"Digital Communication Systems*," John Wiley and Sons, New Delhi, Forth Edition, 2014.
3. H. Taub, D. Schlling, and G. Saha, "*Principles of Communication Systems,*" Tata Mc-Graw Hill, New Delhi, Third Edition, 2012.
4. Lathi B P, and Ding Z., "*Modern Digital and Analog Communication Systems*," Oxford University Press, Forth Edition, 2009.
5. T L Singal, "*Analog and Digital Communication*," Tata Mc-Graw Hill, New Delhi, First Edition, 2012.
6. P Ramakrishna Rao, *"Digital Communication*," Tata Mc-Graw Hill, New Delhi, First Edition, 2011.
7. M F Mesiya, *"Contempory Communication systems*", Mc-Graw Hill, Singapore, First Edition, 2013.

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of two tests should be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions for 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETC602	Discrete Time Signal Processing	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETC602	Discrete Time Signal Processing	20	20	20	80	-	-	-	100

Course Prerequisite: ETC 405: Signals and System

Course Objectives:

- To develop a thorough understanding of the central elements of discrete time signal processing theory and the ability to apply this theory to real-world signal processing applications.
- Use z-transforms and discrete time Fourier transforms to analyze a digital system.
- Understand the discrete Fourier transform (DFT), its applications and its implementation by FFT techniques.
- Design and understand finite & infinite impulse response filters for various applications.
- The course is a prerequisite course for further studying of other multimedia related courses, such as speech processing, image processing, audio and video data compression, pattern recognition, communication systems and so forth.

Course Outcomes: Student will able to

- Formulate engineering problems in terms of DSP tasks
- Apply engineering problem solving strategies to DSP problems
- Design and test signal processing algorithms for various applications
- Recover information from signals
- Design and simulate digital filters

Module No.		Topics	Hrs.
1		**Transform Analysis of Linear Time Invariant System**	04
	1.1	Review of *Z* transform and its properties, response to sinusoidal and complex exponential signals, steady-state response to periodic input signals, response to aperiodic input signals, relationships between the system function and the frequency response function, computation of the frequency response function	
	1.2	LTI systems as frequency-selective filters like; low pass, high pass, band pass, notch, comb, all-Pass filters, and digital resonators.	
	1.3	Invertibility of LTI systems, minimum-phase, maximum-phase, mixed-phase systems	

2		**The Discrete Fourier Transform and Efficient Computation.**	**12**
	2.1	Frequency domain sampling and reconstruction of discrete time signals, discrete Fourier transform (DFT), DFT as a linear transformation, properties of the DFT, relationship of the DFT to other transforms	
	2.2	Fast Fourier Transform: Radix-2 and split-radix fast Fourier transform (FFT) algorithms and their applications	
	2.3	Quantization effects in the computation of the DFT	
3		**Design of Digital filters and Implementation**	**12**
	3.1	Design of Infinite Impulse Response (IIR) filters using impulse invariant method and bilinear transformation method, Butterworth and Chebyshev filter approximation.	
	3.2	Concepts of Finite Impulse Response (FIR) filter, symmetric and anti symmetric FIR filter, FIR filter design using window method and frequency sampling method.	
	3.3	Realization structures for IIR and FIR filters using direct form structures, cascade, parallel structures, and lattice, ladder structure (only conceptual understanding)	
4		**Multi rate Signal Processing**	**08**
	4.1	Decimation by a factor *D*, interpolation by I, sampling rate conversion by a rational factor I/D	
	4.2	Polyphase filter structures, interchange of filers and down samplers/up samplers, sampling rate conversion with cascade integrator comb filters, polyphase structures for decimation and interpolation filters, structures for rational sampling rate conversion	
	4.3	Multistage implementation of sampling rate conversion.	
	4.4	Sampling rate conversion of band pass signals	
	4.5	Sampling rate conversion by an arbitrary factor – arbitrary re-sampling with polyphase interpolators, narrow band filter structures.	
	4.6	Application of Multirate Signal Processing for design of phase shifters, interfacing of digital systems with different sampling rates, implementation of narrowband low pass filters, sub band coding of speech signals	
5		**Analysis of Finite Word length effects**	**08**
	5.1	Quantization process and errors, quantization of fixed-point numbers, quantization of floating-point numbers, analysis of coefficient quantization effects	
	5.2	A/D Conversion Noise Analysis, Analysis of Arithmetic Round-Off Errors and dynamic range scaling	
6		**Applications of Digital Signal processing:**	**08**
	6.1	Dual –Tone multi frequency signal detection, spectral analysis of sinusoidal signals, spectral analysis of non stationary signals, and spectral analysis of random signals	
	6.2	Musical sound processing, digital music synthesis, discrete time analytic signal generation.	
	6.3	Trans-multiplexers, oversampling ADC and DAC and sparse antenna array design	
Total			**52**

Recommended Books:

1. Alan V. Oppenheim and Ronald Schafer, "*Discrete Time Signal Processing*", Pearson Education
2. J. Proakis, D. G. Manolakis, and D. Sharma, "*Digital Signal Processing: Principles, Algorithms and Applications*", Pearson Education.
3. P.P. Vaidyanathan, "*Multirate Systems and Filter Banks*", Pearson.
4. Robert Schilling and Sandra Harris, "*Fundamentals of Digital Signal Processing using MATLAB"*, Cengage Learning.
5. Sanjit K.Mitra, "*Digital Signal Processing*", McGrawHill education

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of two tests should be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions for 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules

Course Code	Course Name	Teaching Scheme	Credits Assigned					
		Theory	Practical	Tutorial	Theory	TW/ Practical	Tutorial	Total
ETC603	Computer Communication Networks	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETC603	Computer Communication Networks	20	20	20	80	-	-	-	100

Course pre requisite: ETC 502 Analog Communication

Course Objective:

- To introduce analysis and design of computer and communication networks.
- To understand the network layered architecture and the protocol stack.

Course Outcomes:

Upon completion of the subject, students will be able to:

- Assemble the components of a PC and install one or more network operating systems resulting in a functioning
- Design a small or medium sized computer network including media types, end devices, and interconnecting devices that meets a customer's specific needs.
- Perform basic configurations on routers and Ethernet switches.
- Demonstrate knowledge of programming for network communications
- Learn to simulate computer networks and analyze the simulation results
- Troubleshoot connectivity problems in a host occurring at multiple layers of the OSI model
- Develop knowledge and skills necessary to gain employment as computer network engineer and network administrator.

Module No.		Topics	Hrs.
1.		**Network Architectures, Protocol layers, and their Service Models:**	04
	1.1	OSI-RM model and TCP/IP protocol	
2		**Principles of Network Applications:**	10
	2.1	Application layer protocols such as HTTP, FTP, and SMTP.	
	2.2	Peer-to-Peer File Sharing Protocols and Architectures	
	2.3	ISPs and Domain name systems, Socket API and network socket programming	

3	**3.1**	**Reliable and Unreliable Transport-layer protocols:**	**10**
	3.2	TCP and UDP, Port numbers, Multiplexing and de-multiplexing	
	3.3	Flow control and congestion control. fairness delay, jitter, and loss in packet-switched networks	
	3.4	Bandwidth, throughput, and quality-of-service	
4	**4.1**	**Network layer Services and Protocols**	**10**
	4.2	Switching fabric, routing and forwarding, queues and buffering	
	4.3	Virtual-circuit and datagram networks, internet protocol. IPv4 and IPv6 tunneling	
	4.4	Link State and Distance Vector algorithms, Routing in the Internet RIP, OSPF, and BGP	
	4.5	Broadcast and multicast, handling mobility	
5		**Data link layer Services and Protocols:**	**10**
	5.1	Link-layer and its services, Ethernet, hubs, bridges, and switches	
	5.2	Link-layer addressing, ATM and MPLS	
	5.3	Local area networks and IEEE 802.11 wireless LANs, multiple-access protocols. Random access, efficiency of pure and slotted ALOHA, CSMA, CSMA/CD, and CSMA/CA	
6		**Introduction to Physical-layer Services and Systems**	**08**
	6.1	Introduction to physical media, Coax, fiber, twisted pair, DSL, HFC, WiMax, cellular, satellite, and telephone networks, bit transmission, frequency division multiplexing. time division multiplexing	
Total			**52**

Recommended Books:

1. Andrew Tanenbaum, *"Computer Networks",* PHI New Dehli,
2. Natalia Olifer and Victor Olifer, " Computer Networks", Wiley India,New Delhi
3. J. F. Kurose and K. W. Ross, "*Computer Networking: A Top-Down Approach*", Pearson Publication , 5th Edition, March 2009
4. L.Garcia et al, "*Communication Networks*", McGraw Hill Publication, 2nd Edition
5. B. Forouzan, "*Data Communication and Networking*", McGraw Hill Publication, 5th edition.

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of two tests should be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3 Question No.1 will be compulsory and based on entire syllabus wherein sub questions for 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules.

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETC 604	Television Engineering	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETC 604	Television Engineering	20	20	20	80	-	-	-	100

Pre requisite : ETC 502 Analog Communication

Course Objective:

- To introduce the basics of picture transmission and reception.
- To become well conversant with new development in video engineering.
- To introduce most latest and revolutionary ideas in the field of digital TV, HDTV, WDTV.

Course outcome: The students will be able to

- Describe and differentiate working principles of latest digital TV, HDTV, WDTV.
- Understand, use and working principles of latest display like LCD, LED, Plasma and large plat panel monitors

Module No.		Topics	Hrs.
1		**Fundamentals of Analog T V system**	**10**
	1.1	Transmitter and receiver- block diagram approach, interlaced scanning, composite video signal, VSB transmission and reception (CCIR-B standards)	
	1.2	Camera tubes: basic principle ,Vidicon and Image orthicon	
2		**Color T V**	
	2.1	Compatibility considerations, Color theory, chromaticity diagram, generation of color TV signals, luminance signal, chrominance signal, frequency interleaving process, color subcarrier frequency.	**10**
	2.2	NTSC system- transmitter and receiver, PAL system- transmitter and receiver	
3		**Fundamental Concept of Digital Video**	
	3.1	Digitization, pixel array, scanning notation, viewing distance and angle, aspect ratio, frame rate and refresh rate.	**12**
	3.2	Raster scanning, scan line waveform, interlace, scanning standards.	
	3.3	Sync structure, data rate, linearity, bandwidth and data rate, resolution, luma, color difference coding, chroma sub sampling	
	3.4	Component digital video, composite video	

4		**Advanced TV systems**	**6**
	4.1	Digital video and audio signals	
	4.2	MAC signal, D2-MAC/packet signal, MAC decoding and interfacing, advantages of MAC signal	
	4.3	Direct-to-home TV(DTH)	
5		**High definition televisions**	**8**
	5.1	High definition TV systems, HDTV standards and compatibility, resolution and working.	
	5.2	Wide dimensions high definition TV	
	5.3	Standards of wide dimensions HDTV	
	5.4	MUSE system	
6		**Displays**	**6**
	6.1	Principle, working, advantages and disadvantages of Plasma, LED,LCD	
Total			**52**

Recommended Books:

1. Gulati R.R, " *Monochrome and Color Television*," Wiley Eastern Limited publication.
2. R.G.Gupta , "*Television and Video Engineering*", Tata Mc Graw Hill publication.
3. Dhake A.M, "*Television and Video Engineering*", Tata McGraw Hill publication.
4. Keith Jack, "*Video Demystified*", 4e, , Elsevier
5. Charles Poynton, "*San Francisco, Digital video and HDTV, Algorithms And Interfaces*," Morgan Kaufmann publishers, 2003.
6. Stan Prentiss, *"High Definition TV*", second edition, , Tata McGraw Hill publication

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of two tests should be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions for 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETC 605	Operating System	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETC 605	Operating System	20	20	20	80	-	-	-	100

Course Pre-requisite: Basic concepts of computer systems

Course Objectives:

- To introduce operating system as a resource manager, its evolutions and fundamentals.
- To help student understand concept of process and different process (linear and concurrent) Scheduling policies.
- To help student familiar with memory, file and I/O management policies.

Course Outcomes: On completing this course Student will able to:

- Understand the role of an operating system, its function and issues.
- Compare between different algorithms used for management and scheduling of processes, Memory and input-output operation.
- Appreciate the role of various productivity enhancing tools.

Module No.		Topics	Hrs.
1		**Fundamental of Operating System(OS)**	06
	1.1	Definition, objectives, functions, evolution, services, types, and different views of OS	
	1.2	Operating System as a resource manager, system calls, and shell	
	1.3	Monolithic systems, layered systems, client server model, monolithic kernel and microkernel	
2		**Process Management and Memory Management**	10
	2.1	Process, process creation, process control block, process states, process state transition diagram	
	2.2	Scheduling queues and schedulers, preemptive and non- preemptive scheduling algorithms, types of threads, multithreading models	
	2.3	Race condition, critical section, mutual exclusion, semaphores, monitors	
	2.4	Multiprogramming with fixed and variable partitions, memory allocation strategies	
	2.5	Logical and physical address space, paging and segmentation	
	2.6	Concept, performance of demand paging, page replacement algorithms.	
	2.7	Deadlock Problem, deadlock characterization, deadlock prevention and deadlock avoidance deadlock detection and recovery	

3		**File Management and Input Output Management**	**10**
	3.1	File Naming, File Structure, File Types, File Access, File Attributes, File Operations, Memory Mapped Files, Implementing Files, contiguous allocation, linked list allocation, indexed allocations, Inode	
	3.2	Single level directory system, Two level directory system, Hierarchical Directory System	
	3.3	Principles of Input/output H/W: I/O Devices, Device Controllers, Direct Memory Access.	
	3.4	Principles of Input/output S/W: Goals Of I/O S/W, Interrupt Handler, Device Driver, Device Independent I/O Software	
	3.5	Disks : RAID levels, Disks Arm Scheduling Algorithms	
	3.6	Management of free blocks.	
4		**Unix Operating System**	06
	4.1	History of UNIX, UNIX Goals, Unix Shell, interfaces to Unix, UNIX utility programs	
	4.2	Traditional UNIX Kernel, Modern UNIX Systems	
	4.3	Unix process management: Concept, Scheduling in Unix	
	4.4	Unix Memory management: Paging, Page replacement strategies	
	4.5	Unix file management: I-node, File allocation, I/O management	
	4.6	Unix Security measures	
5		**Linux Operating System**	10
	5.1	History, Linux Processes and Thread management	
	5.2	Scheduling in Linux, Linux System calls	
	5.3	Memory management: Virtual memory, Buddy Algorithm, Page replacement policy	
	5.4	Linux File System	
	5.5	I/O management: Disk Scheduling	
	5.6	Advantages of Linux and Unix over Windows	
6		**Real Time Operating System(RTOS)**	**10**
	6.1	Introduction, Characteristics of real-time operating systems	
	6.2	Real Time task Scheduling, Modeling Timing constraints, Table-driven scheduling	
	6.3	Cyclic schedulers	
	6.4	Earliest Deadline First (EDF) scheduling	
	6.5	Rate Monotonic Algorithm(RMA)	
Total			**52**

Recommended Books:

1. Tanenbaum, "*Modern Operating Systems*", III[rd] Edition, PHI
2. Silberschatz A., Galvin P., and Gagne G, "*Operating Systems Concepts*", VIII[th] Edition Wiley.
3. William Stallings, "*Operating System-Internal & Design Principles*", VI[th] Edition, , Pearson
4. Rajib Mall, "*Real-Time Systems: Theory and Practice*," Pearson, 2008.
5. Maurice J. Bach, "*The Design of Unix Operating System*", Prentine Hall
6. Achyut S. Godbole, "*Operating Systems*", 2nd edition, Tata McGraw Hill
7. Richard Blum and Christine Bresnahan, "*Linux Command Line & Shell Scripting*", 2nd edition, Wiley

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of two tests should be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions for 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules.

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETC606	VLSI Design	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
ETC606	VLSI Design	20	20	20	80	--	--	--	100

Course Pre-requisite:

- ETC303: Digital Electronics
- ETC302: Analog Electronics-I
- ETC402: Analog Electronics-II
- ETC505: Integrated Circuits

Course Objectives:

- To teach fundamentals of VLSI circuit design and implementation using circuit simulators and layout editors.
- To highlight the circuit design issues in the context of VLSI technology.

Course Outcomes: After successful completion of the course student will be able to

- Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
- Design MOSFET based logic circuit
- Draw layout of a given logic circuit
- Realize logic circuits with different design styles
- Demonstrate an understanding of working principle of operation of different types of memories
- Demonstrate an understanding of working principles of clocking, power reduction and distribution

Module No.		Topics	Hrs.
1		**MOSFET Fabrication and Scaling**	08
	1.1	**Fabrication:** Fabrication process flow for NMOS and CMOS, CMOS Latch-up	
	1.2	**MOSFET Scaling:** Types of scaling, short channel effects, Level 1 and Level 2 MOSFET Models	
	1.3	**Layout:** Lambda based design rules, MOSFET capacitances	
2		**MOSFET Inverters**	10
	2.1	**Circuit Analysis:** Static and dynamic analysis (Noise, propagation delay and power dissipation) of resistive load and CMOS inverter. Comparison of all types of MOS inverters. Design of CMOS inverters and its layout.	
	2.2	**Logic Circuit Design:** Analysis and design of 2-I/P NAND and NOR using equivalent CMOS inverter.	
3		**MOS Circuit Design Styles**	10
	3.1	**Design Styles:** Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Domino, NORA, Zipper, C^2MOS	
	3.2	**Circuit Realization:** SR Latch, JK FF, D FF, 1 Bit Shift Register, MUX, Decoder using above design styles and their layouts	

4		**Semiconductor Memories**	**08**
	4.1	**SRAM:** ROM Array, SRAM (operation, design strategy, leakage currents, read/write circuits), DRAM (Operation 3T, 1T, operation modes, leakage currents, refresh operation, Input-Output circuits), Flash (mechanism, NOR flash, NAND flash), layout of SRAM and DRAM	
	4.2	**Peripheral Circuits:** Sense Amplifier, Decoder	
5		**Data Path Design**	**08**
	5.1	**Adder:** Bit adder circuits, Ripple carry adder, CLA adder	
	5.2	**Multipliers and shifter:** Partial-product generation, partial-product accumulation, final addition, Barrel Shifter	
6		**VLSI Clocking and System design**	**08**
	6.1	**Clocking:** CMOS clocking styles, Clock generation, stabilization and distribution	
	6.2	**Low Power CMOS Circuits:** Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling.	
	6.3	**IO pads and Power Distribution:** ESD protection, Input circuits, Output circuits, Simultaneous switching noise, power distribution scheme	
	6.4	**Interconnect:** Interconnect delay model, interconnect scaling and crosstalk	
Total			**52**

Recommended Books:

1. Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition, 2012.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.
3. John P. Uyemura, "*Introduction to VLSI Circuits and Systems*", Wiley, Student Edition, 2013.
4. Neil H. E. Weste, David Harris and Ayan Banerjee, "*CMOS VLSI Design: A Circuits and Systems Perspective*", Pearson Education, 3rd Edition.
5. R. Jacob Baker, "*CMOS Circuit Design, Layout and Simulation*", Wiley, 2nd Edition, 2013

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of two tests should be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions for 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules.

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETL601	Discrete Time Signal Processing	--	02	--	--	01	--	01

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical and Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETL601	Discrete Time Signal Processing	--	--	--	--	25	25	-	50

Term Work:
At least ten experiments covering entire syllabus of ETC 602:Discrete Time Signal Processing on should be set to have well predefined inference and conclusion. The experiments should be student's centric and attempt should be made to make experiments more meaningful, interesting and innovative. Term work assessment must be based on overall performance of the student with every experiment graded. The grade must be converted to marks as per credit and grading system manual, and should be added and average. Base on above scheme grading and term work assessment should be done.
Practical and oral examination will be based on entire syllabus.

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETL602	Communication Engineering Laboratory III	--	02	--	--	01	--	01

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical and Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETL602	Communication Engineering Laboratory III	--	--	--	--	25	25	-	50

Term Work:
At least ten experiments covering entire syllabus for ETC 601: Digital Communication and ETC 603 Computer Communication and Networks should be set to have well predefined inference and conclusion. The experiments should be student's centric and attempt should be made to make experiments more meaningful, interesting and innovative. Term work assessment must be based on overall performance of the student with every experiment graded. The grade must be converted to marks as per credit and grading system manual, and should be added and average. Base on above scheme grading and term work assessment should be done.
Practical and oral examination will be based on entire syllabus of ETC 601 and ETC 603

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETL604	Communication Engineering Laboratory IV	--	02	--	--	01	--	01

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical and Oral	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
ETL604	Communication Engineering Laboratory -IV	--	--	--	--	25	25	-	50

Term Work:
At least six experiments covering entire syllabus for ETC 606:VLSI Design and minimum four experiments for ETC 604: Television Engineering. should be set to have well predefined inference and conclusion. The experiments should be student's centric and attempt should be made to make experiments more meaningful, interesting and innovative. Term work assessment must be based on overall performance of the student with every experiment graded. The grade must be converted to marks as per credit and grading system manual, and should be added and average. Base on above scheme grading and term work assessment should be done.
Practical and oral examination will be based on entire syllabus for ETC 606 and ETC 604.

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETL605	Mini Project II	--	02	--	--	01	--	01

Course Code	Course Name	Examination Scheme						
		Theory Marks				Term Work	Practical/ Oral	Total
		Internal assessment			End Sem. Exam			
		Test 1	Test 2	Ave. Of Test 1 and Test 2				
ETL605	Mini Project II	--	--	--	--	25	25	50

Term Work:

The main intention of Mini Project is to make student enable to apply the knowledge and skills learned out of courses studied to solve/implement predefined practical problem. The students undergo various laboratory/tutorial/simulation laboratory/work shop courses in which they do experimentation based on the curriculum requirement. The mini Project may be beyond the scope of curriculum of courses taken or may be based on the courses but thrust should be on

- Learning additional skills
- Development of ability to define and design the problem and lead to its accomplishment with proper planning.
- Learn the behavioral science by working in a group

The group may be maximum **four** (04) students. Each group will be assigned one faculty as a supervisor. The college should keep proper assessment record of progress of the project and at the end of the semester it should be assessed for awarding TW marks. The TW may be examined by approved internal faculty appointed by the head of the institute. The final examination will be based on demonstration in front of internal and external examiner. In the examination each individual student should be assessed for his/her contribution, understanding and knowledge gained about the task completed.

The topic of Mini Project I and II may be different and / or may be advancement in the same topic. The students may use this opportunity to learn different computational techniques as well as some model development. This they can achieve by making proper selection of Mini Projects.