Q.1(a) Explain Resolution, Accuracy and settling time w.r.t. DAC. **05**

Ans.: **Resolution :**

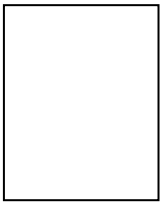
It is described as the smallest possible change in the analog output voltage. Its value depends upon the no. of bits in the digital input applied to DAC. Higher the number of bits, higher is the resolution.

Accuracy : It indicates how close the analog output voltage is to its theoretical value. It indicates deviation of actual output from its theoretical value.

Settling Time : The time required to settle the analog output within 1/2 LSB of the final value, after the change in digital input is called as settling time.

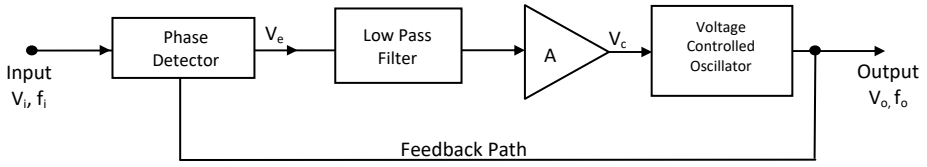
Q.1(b) Compare Voltage regulators with IC78XX and IC723. **05**

Ans.:

	IC78XX	**IC723**
1.	Fixed positive voltage regulator series.	It is variable voltage regulator
2.	It is a 3 pin IC.	It is a 14 pin IC.
3.	The voltages available in series are 5, 6, 8, 12, 15, 18 & 24 volts.	Output voltage can be adjusted between 2 to 37 volts.
4.	Maximum output current is 1 mA	Maximum load current is 150 mA.
5.	Pin Connections 	Pin Connections 

Q.1(c) Describe the basic block diagram of Phase Locked Loop (PLL). **05**

Ans.:



Basic Block Diagram of PLL

Operation of a PLL :

1. **Phase Detector/Comparator :** The two inputs to a phase detector or comparator are the input voltage ν_i at frequency f_i and the feedback voltage from a voltage controlled oscillator (V_{CO}) at a frequency f_0.
   The phase detector compares these two signals and produces a dc voltage V_c which is proportional to the phase difference between f_i and f_0. The output voltage V_c of

the phase detector is called as "error" voltage. This error voltage is then applied to Low pass filter.

2. **Low Pass Filter :** The low pass filter removes the high frequency noise present in the phase detector output and produces a ripple free dc level.
   This dc level is amplified to an adequate level and applied to the voltage controlled oscillator. The dc amplifier output voltage is called as control voltage V_c.
3. **Voltage Controlled oscillator (v_{CO}) :** The control voltage V_c is applied at the input of V_{CO}. The output frequency of V_{CO} is directly proportional to the dc control voltage V_c. The V_{CO} frequency "f_o" is compared with the input frequency "f_i" by the phase detector and it (V_{CO} frequency) is adjusted continuously until it is equal to the input frequency "f_i" i.e. $f_o = f_i$.

Q.1(d) Define input Offset voltage, Output Offset voltage, Input bias current and input offset current for Op–amps. 05

Ans.: **Input Offset voltage :** It is voltage that must be applied between the two input terminals of op–amp to null the output. For IC 741 it is 6 mV.

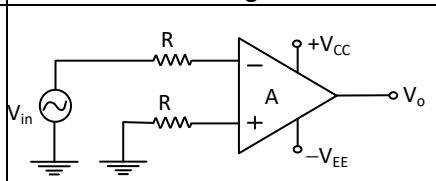
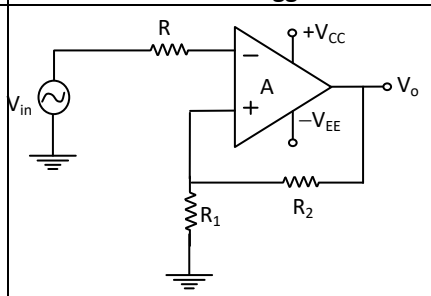
Output offset voltage : In op–amp when the input is zero, the output is also expected to be zero. However because of the effect of the input offset voltage and current, the output is significantly larger. This is called output offset voltage I V = VOOT

Input Bias current : It is the average of the base currents entering into the terminals of op–amps. For IC 741 it is 500 mA.

Input offset current : The algebraic difference between the base current flowing through terminals of op-amp for IC741 it is 200 mA.

Q.1(e) Compare Zero Crossing Detector with Schmitt Trigger. 05

Ans.:

	Zero Crossing Detector	Schmitt Trigger
i)		
ii)	It has only one reference voltage	It has two reference voltages [V_{UTP} and V_{LTP}]
iii)	The input voltage is applied to inverting terminal and fixed voltage to non-inverting terminal or vice versa.	The input voltage is applied to inverting terminal and feedback voltage to the non-inverting input
iv)	It is open loop system	It is closed loop system

v)	It doesn't exhibits hysteresis	Schmitt Trigger exhibits hysteresis characteristics
vi)	It is used as level detector or phase detector	It is used as a wave shaping circuit, level detector, pulse height discriminator. Its main use to convert any kind of wave into square wave.
vii)	In this transition occurs at only one level	In this transition occurs at two level.

Q.2(a) Derive the Output Voltage (V_0) expression of Op–amp three input Averaging Circuit. **10**

Ans.:

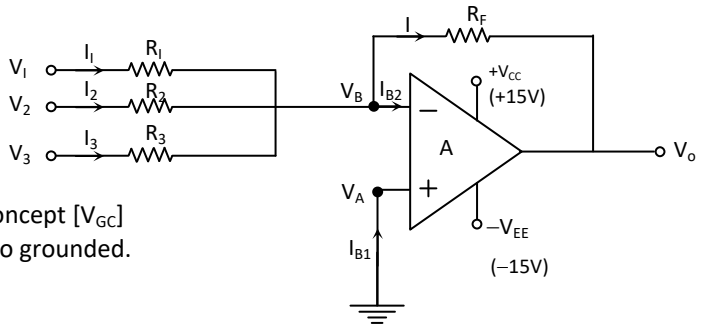


Fig.: Three input averaging amplifier.

According to virtual ground concept [V_{GC}]

V_A is grounded ∴ V_B is also grounded.

According to NIBCC

$$I_{B1} = I_{B2} = 0$$

$$\therefore \quad I = [I_1 + I_2 + I_3]$$

$$\therefore \quad \frac{-V_o}{R_F} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$\therefore \quad \frac{V_o}{R_F} = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

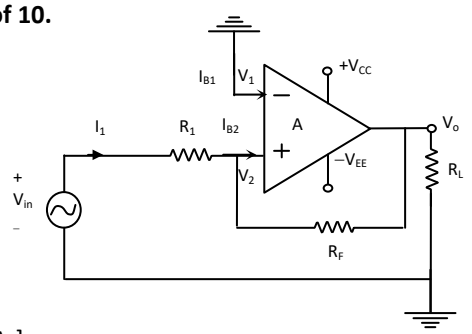
$$\therefore \quad V_o = -\left[\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right] \qquad \ldots(1)$$

For averaging amplifier, If $R_1 = R_2 = R_3 = R$ and $R_F/R = 1/3$ then equation (1) becomes

$$\therefore \quad V_o = -\left[\frac{(V_1 + V_2 + V_3)}{3}\right]$$

Q.2(b) Give Complete Analysis of Inverting Amplifier Op–amp circuit. Hence design it for Voltage gain of 10. **10**

Ans.:



(1) Voltage gain [A_F]

Since $I_B = 0$ ∴ $I_1 = I_2$

$\therefore \quad \frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_F}$ $\quad \{\because V_{id} = V_1 - V_2 = -V_2$ (because $V_1 = 0$)

$$A = \frac{V_o}{V_{id}} = \frac{V_o}{-V_2} \quad \therefore \ V_2 = \frac{V_o}{A}\}$$

$$\therefore \quad \frac{V_{in}}{R_1} + \frac{V_o}{AR_1} = -\frac{V_o}{R_F} - \frac{V_o}{AR_F}$$

$$\therefore \quad \frac{V_{in}}{R_1} = -V_o\left[\frac{1}{AR_1} + \frac{1}{R_F} + \frac{1}{AR_F}\right]$$

$$\therefore \quad = -V_o\left[\frac{R_F + AR_1 + R_1}{AR_1R_F}\right]$$

$$\therefore \quad \frac{V_o}{V_i} = -\frac{1}{R_1} \cdot \frac{AR_1R_F}{R_F + AR_1 + R_1}$$

$$\therefore \quad A_F = \frac{-AR_F}{R_F + AR_1 + R_1} \quad \Rightarrow \text{ exact gain}$$

Normally, $AR_1 >> R_1 + R_F$

$$\therefore \quad A_F = \frac{-AR_F}{AR_1} = -\frac{R_F}{R_1}$$

(2) Input Resistance [R_{IF}]

Millerising resistance R_F

$$R_{mi} = \frac{R_F}{1 + A}$$

$$\& \quad R_{mo} = R_F \frac{A}{1 + A}$$

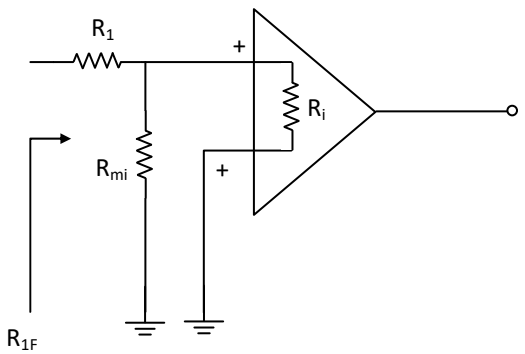
From the diagram,

$$R_{IF} = R_1 + \left[R_{mi} \,||\, R_i\right]$$

$\because \ R_{mi} = \frac{R_F}{1 + A}$ and A is very high

$\therefore \quad R_{mi} \cong 0$

$\therefore \quad R_{IF} = R_1$



(3) Output Resistance [R_{OF}]

$I_B \cong 0 \quad \therefore I_o = I_A$

Applying KVL to figure (2)

$V_o - I_oR_o - AV_{id} = 0$

$$\therefore \quad I_o = \frac{V_o - AV_{id}}{R_o}$$

$$= \frac{V_o - A(V_1 - V_2)}{R_o}$$

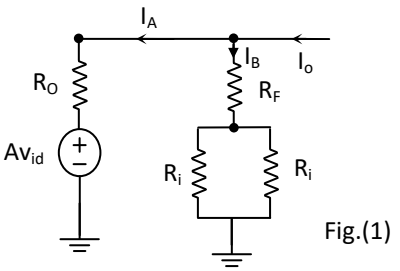


Fig.(1)

$$I_o = \frac{V_o + AV_2}{R_o} = \frac{V_o + AV_E}{R_o} = \frac{V_o + A\beta V_o}{R_o}$$

$$\therefore \quad \frac{I_o}{V_o} = \frac{1 + A\beta}{R_o}$$

$$\therefore \quad R_{oF} = \frac{V_o}{I_o} = \frac{R_o}{1 + A\beta}$$

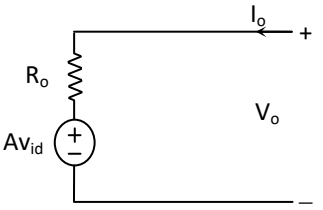


Fig.(2)

For Voltage Gain of 10

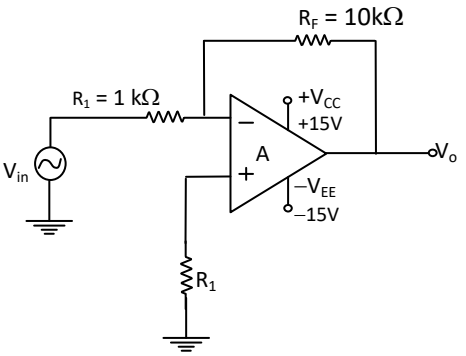
Select IC741 op–amp working at
IV_{CC} = ±15V and ± V_{sat} = ± 12V,
A = 10(given)

We know that, $|A| = \left|\frac{-R_F}{R_1}\right| \quad \Rightarrow 10 = \frac{-R_F}{R_1}$

$\therefore \quad R_F = 10\ R_1$

Let R_1 = 1 kΩ

$\therefore \quad R_F$ = 10 kΩ



Q.3(a) Design Schmitt trigger to achieve UTP = 2 V and LTP = –2 V **10**

Ans.: Given **:** UTP = 2 V, LTP = −2 V

$$UTP = \frac{R_1}{R_1 + R_2} \times V_{sat}^{+}$$

$$LTP = \frac{R_1}{R_1 + R_2} \times V_{sat}^{-}$$

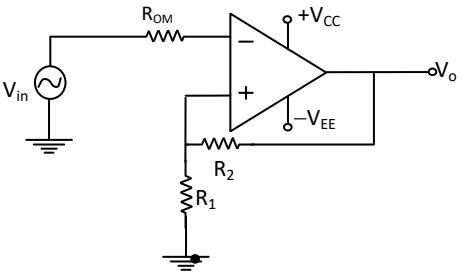
Select IC741 op–amp working at dual power supply of ±15 V and saturation voltage of ± 14 volts.

$$UTP = \frac{R_1}{R_1 + R_2} \times V_{sat}^{+}$$

$$\therefore \quad 2V = \frac{R_1}{R_1 + R_2} \times 14$$

Assume R_1 = 10 kΩ ∴ R_2 = 60 kΩ

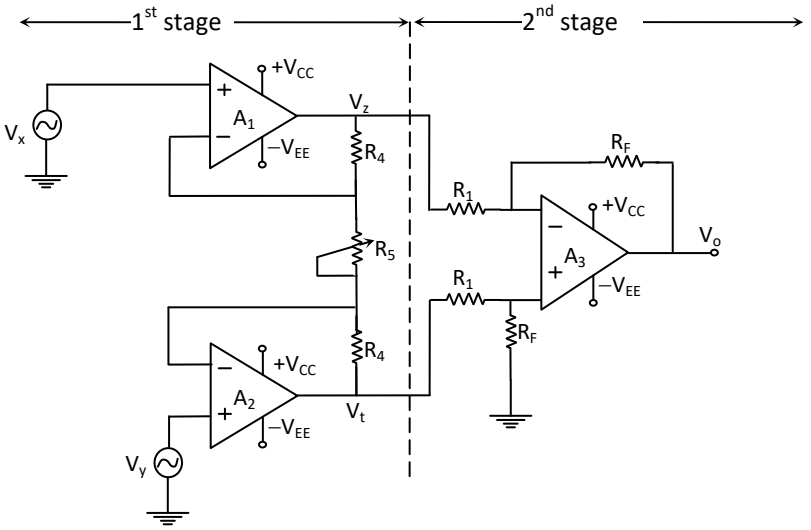
Select R_2 = 62 kΩ



Schmitt Trigger

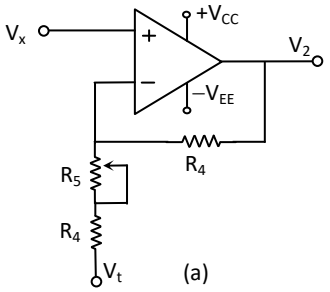
Q.3(b) **Draw neat diagram of Instrumentation Amplifier using Op–amp and hence derive the equation of output voltage.** **10**

Ans.:

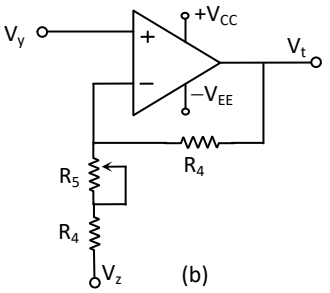


→ 1st stage is composed two op–amps A_1 and A_2, while the 2nd is formed by op–amp A_3. Therefore to find overall gain A_0 of the amplifiers, voltage gain of each stage should be determined.

→ The 1st stage can be viewed as two separate differential amplifiers as shown in the figure (a) and (b) below.



(a)



(b)

$$\therefore \quad V_z = \left[1 + \frac{R_4}{R_4 + R_5}\right] V_x - \left[\frac{R_4}{R_4 + R_5}\right] V_t$$

$$\therefore \quad V_z = \left[\frac{2R_4 + R_5}{R_4 + R_5}\right] V_x - \left[\frac{R_4}{R_4 + R_5}\right] V_t \qquad \ldots(1)$$

$$\text{And } V_t = \left[1 + \frac{R_4}{R_4 + R_5}\right] V_y - \left[\frac{R_4}{R_4 + R_5}\right] V_z$$

$$\therefore \quad V_t = \left[\frac{2R_4 + R_5}{R_4 + R_5}\right] V_y - \left[\frac{R_4}{R_4 + R_5}\right] V_z \qquad \ldots(2)$$

The output of 1st stage is ,

$$V_{zt} = V_z - V_t$$

$$V_{zt} = \left[\frac{2R_4 + R_5}{R_4 + R_5}\right](V_x - V_y) + \left[\frac{R_4}{R_4 + R_5}\right](V_x - V_t)$$

$$V_{zt} \times \left[\frac{1 - R_4}{R_4 + R_5}\right] = \left[\frac{2R_4 + R_5}{R_4 + R_5}\right](V_{xy})$$

$$V_{zt}\left[\frac{R_5}{R_4 + R_5}\right] = \left[\frac{2R_4 + R_5}{R_4 + R_5}\right]V_{xy}$$

$$\frac{V_{zt}}{V_{xy}} = \left[\frac{2R_4 + R_5}{R_5}\right]$$

Gain of 2nd stage is $\frac{V_o}{V_{zt}} = \frac{-R_F}{R_1}$

$\therefore$ Overall gain = $\frac{V_{zt}}{V_{xy}} \times \frac{V_o}{V_{zt}} = \left[\frac{2R_4 + R_5}{R_5}\right]\left[\frac{-R_F}{R_1}\right]$

$\therefore$ $\frac{V_o}{V_{xy}} = \left[\frac{-R_F}{R_1}\right]\left[\frac{2R_4 + R_5}{R_5}\right]$

Q.4(a) Explain the working of R/2R Ladder D/A converter **10**

Ans.:

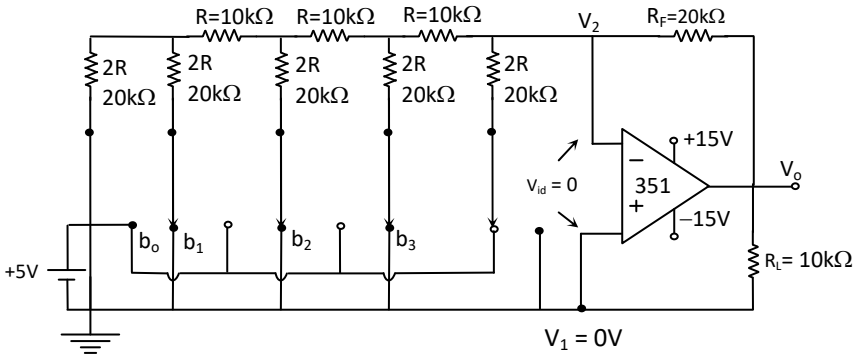


Fig.(a) : D/A Converter with R/2R resistor

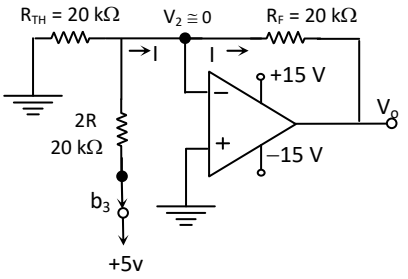


Fig.(b): Equivalent circuit when b_3 is high and b_0, b_1 & b_2 are low.

- The figure above shows a D/A converter with R and 2R resistors.
- The binary inputs are simulated by switches b_0 through b_3 and the output is proportional to the binary inputs.
- Binary inputs can be either the high (+5 V) or low (0 V).
- Assume the most significant bit (MSB) b_3 is connected to +5 V and other switches are connected to ground.
- Thevenizing the circuit to the left of the switch b_3 Thevenin's equivalent resistance R_{TH} is ,

  R_{TH} = [{(2R || 2R + R) || 2R] + R} || 2R] +R

  = 2R = 20 kΩ
- The resultant circuit is shown in figure (b). In this figure, (–) input is a virtual ground ($V_2 \cong 0$), ∴ current through R_{TH} is zero. However current through 2R connected to +5 V is $\frac{5}{20} = 0.25\,\text{mA}$
- The same current flows through R_F and in turn produces output voltage

  V_o = –(20 k)/0.25 mA

  V_o = – 5V
- Using the same analysis, the output voltage corresponding to all possible combinations of binary inputs can be calculated.
- The maximum or full scale output of –9.375 V is obtained when all the inputs are high.
- The output voltage equation can be written as,

$$V_o = -R_F\left[\frac{b_3}{2R} + \frac{b_2}{4R} + \frac{b_1}{8R} + \frac{b_0}{16R}\right]$$

- The great advantage of DAC is that it requires two set of precision values.
- The following graph is output versus input.

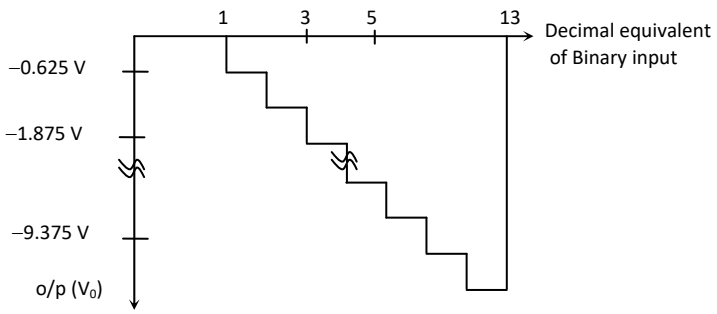


Fig.(c) : Output Versus Input

Q.4(b) Design a 2nd order KRC filter (LPF) for cut off frequency of f_0 = 10KHz with quality factor Q of 5. **10**

Ans.:

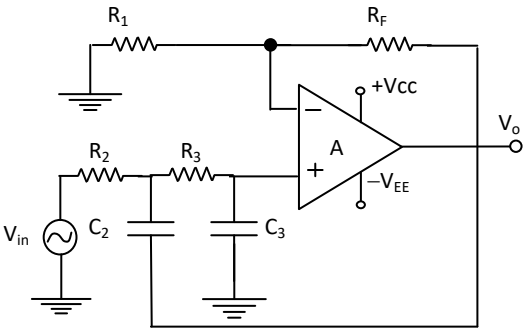


Fig.: Second order KRC filter

Given f_0 = 10 kHz, Q = 5

Design, Let $R_2 = R_3 = R$, $C_2 = C_3 = C$

Assume C = 0.01 μF

For the KRC filter $f_0 = \dfrac{1}{2\pi RC}$

$$\therefore \quad R = \frac{1}{2\pi f_0 C} = \frac{1}{2\pi \times 10 \times 10^3 \times 0.01 \times 10^{-6}}$$

$\therefore$ R = 1.59 kΩ

Select R = 1.5 kΩ, 1/4 watt

Also, $R_F = (k-1)R_1$ …(1)

$$K = 3 - \frac{1}{Q} = 3 - \frac{1}{5}$$

$\therefore$ K = 2.8 …(2)

From (1) and (2)

$R_F = (2.8-1)R_1$

Assume R_1 = 10 kΩ

$\therefore$ R_F = 18 kΩ

Designed circuit will have following components

R_1 = 10 kΩ, $R_2 = R_3$ = 1.5 kΩ, $C_2 = C_3$ = 0.01 μF, R_F = 18 kΩ

Use op–amp IC 741 working on ± 15 V d.c. power supply.

Q.5(a) Explain Astable Multivibrator using Op–amp. **10**

Ans.:

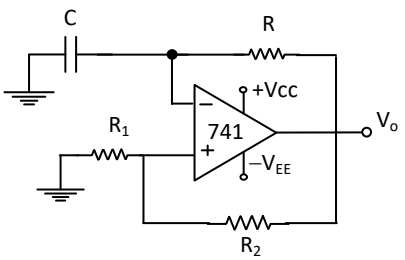


Fig.(a) : Square wave generator

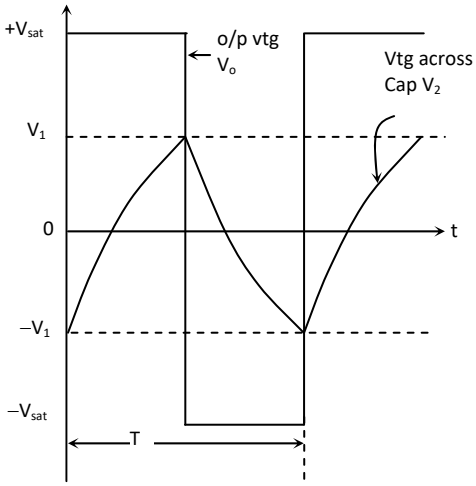


Fig.(b) : Waveform of output voltage and capacitor voltage V_2

- Assume that the voltage across capacitor C is zero volts at the instant the dc supply voltage $+V_{CC}$ and $-V_{EE}$ are applied.
- This means that the voltage at the inverting terminal is zero initially at the same time, voltage V_1 at the non-inverting of a very small finite value that is a function of output offset voltage V_{OOT} and the value of resistors R_1 and R_2.
- Thus the differential input voltage V_{id} is equal to the voltage V_1 at the non-inverting terminal. Although very small voltage V_1 will start to drive op-amp into saturation.
- Suppose that the output offset voltage V_{OOT} is positive and that therefore voltage V_1 is also positive and that therefore voltage V_1 is also positive. Since initially the capacitor C acts as short circuit the gain of op–amp is very large (A); hence V_1 drives the output of op–amp at $+V_{sat}$ (positive saturation).
- With the output voltage of op-amp at $+V_{sat}$, the capacitor C starts charging towards $+V_{sat}$ through resistor R.
- However as soon as voltage V_2 across capacitor C is slightly more positive than V_1, the output of op–amp is forced to negative saturation $-V_{sat}$, the voltage V_1 across R_1 is also negative.

$$V_1 = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

- Thus the net differential voltage $V_{id} = V_1 - V_2$ is negative, which holds the output of op–amp in negative saturation.
- The output remains in negative saturation until the capacitor C discharges and then recharges to a negative voltage slightly higher than $-V_1$.
- Now as soon as capacitor voltage V_2 becomes negative than $-V_1$, the net differential voltage V_{id} becomes positive and hence drives the output of op–amp back to its positive saturation $+V_{sat.}$ This completes one cycle.
- With output at $+V_{sat}$, voltage V_1 at non–inverting input is

$$V_1 = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

- The time period T of the output waveform is given by,

$$T = 2RC\,\ell n\left[\frac{2R_1 + R_2}{R_2}\right]$$

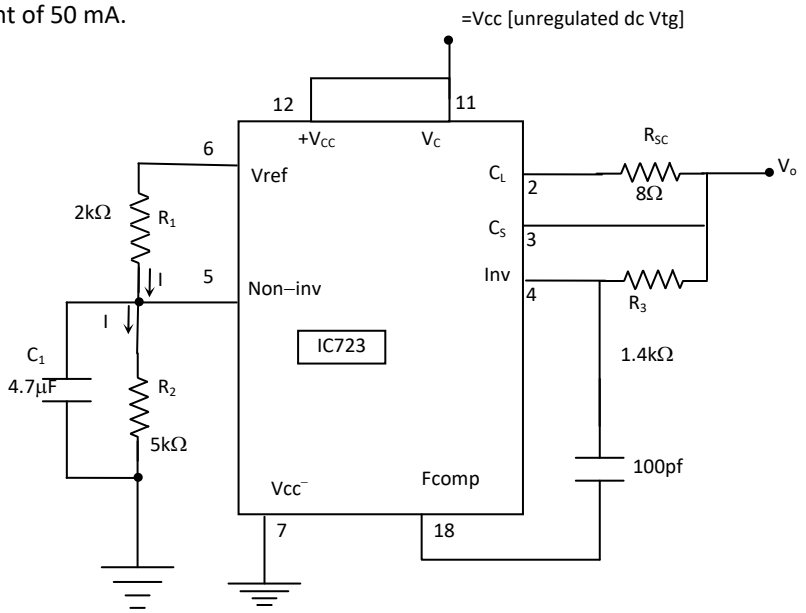
or $$f_o = \frac{1}{2RC\ell n\left[(2R_1 + R_2)/R_2\right]}$$

- This indicates that the frequency of the output f_o is not only a function of the RC time constant but also relationship between R_1 and R_2.
  For e.g. $R_2 = 1.16\ R_1$

$\therefore$ Above equation becomes $f_o = \frac{1}{2RC}$

Q.5(b) Design a positive Voltage regulator to generate V_0 = +5 Volts and I_0 = 50 mA by using IC LM723. Draw neat diagram of the designed circuit. **10**

Ans.: A low voltage and a low current regulator is capable of supplying a load voltage of +5 V and a load current of 50 mA.



given V_0 = 5V

I_0 = 50 mA

Design (i) calculation of Isc

Let Isc = 1.5 x I_0

= 1.5 × 50 mA

Isc = 75 mA

(ii) Calculation of Rsc

$$Rsc = \frac{Vsense}{Isc}$$

Let Vsense = 0.6

$$\therefore Rsc = \frac{0.6}{75\,mA} = 8\Omega$$

Let Rsc = 10Ω Std

(iii) Calculation of R_1 & R_2

Assume current through R_1 & R_2 to be equal to 1mA, as we want the o/p voltage V_0 = 5V, voltage at non–inverting terminal i.e. voltage across R_2 should be 5V.

$$\therefore R_2 - \frac{5V}{1mA} = 5k\Omega$$

Select R_2 = 5.1 k Ω Std

Voltage across R_1 is Vref $-$ V_{R2}

i.e. Vrof $-V_0$ = 7 $-$ 5 = 2 Volts.

$$\therefore R_1 = \frac{2}{1mA} = 2k\Omega$$

Select R_1 = 2.2kΩ std

(iv) To calculate R_3

$$R_3 = R_1 \,||\, R_2 = \frac{R_1 x R_2}{R_1 + R_2} = 1.4\ k\,\Omega$$

Select $R_3 = 1.5k\Omega$ std

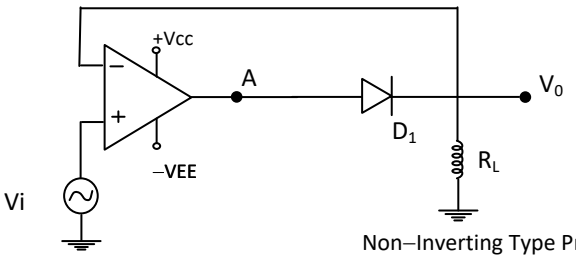
(v) Select C_1 as 4.7 μF/10V, which is an additional filter Capacitor.

(vi) Therefore the Component Values are,

$R_1 = 2.2k\Omega$, $R_2 = 5.1k\Omega$, $R_3 = 1.5k\Omega$, $R_{sc} = 10\Omega$ & $C_1 = 4.7\ \mu F/10V$

Q.6(a) Write short note on Half Wave Precision Rectifier **05**

Ans.:



Non–Inverting Type Precision Half Wave Rectifier.

→ The input Voltage is applied to the non-inverting (+) terminal directly.

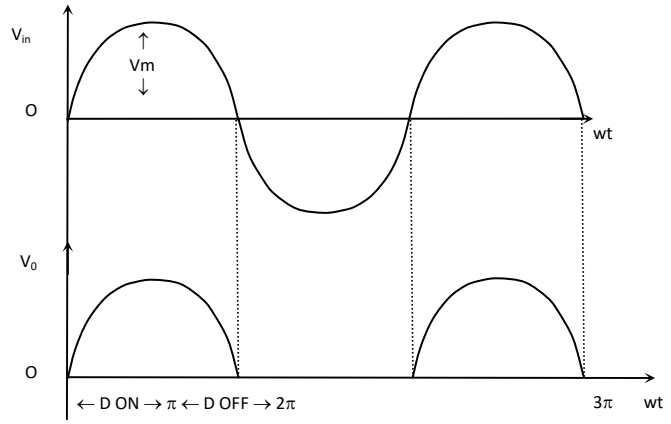
→ In positive half cycle of input, the op–amp, output at point A is positive & high. This will forward biased the diode. As diode is F.B. it acts as low resistance device & the Ckt acts as a Voltage followes.

→ The o/p voltage is positive half cycle is equal to the i/P, voltage.

– Use of high gain op–amp makes it possible to rectify i/P voltages even in the mV range.

– In precission rectifies, the amplitude of i/P v/g required to F.B. diode is [0.7/Av] instead of 0.7V. Av gain of open loop is in order of 2×10^5.

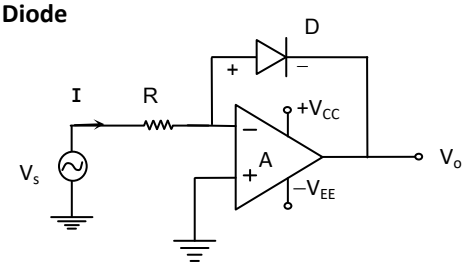
∴ Precision Rectifies can rectify signals with amplitude of mV range.



Input – Output Waveforms Of Precision Rectifier.

Q.6(b) Write short note on Log – Antilog Amplifier using op–amp. **05**

Ans.: Log Amplifier Using Diode



The circuit diagram for log amplifier is as shown in the figure above,
The current through the diode D is given by,

$$I_F = I_s\left[e^{Vf/\eta V_T} - 1\right]$$

Where, I_F = Current through diode
V_f = potential difference across diode
V_T = KT = Voltage equivalent of temperature
I_0 = Reverse current
n = 1 for Ge
= 2 for Si

$$I_F = I_s\ e^{Vf/\eta V_T}$$

$$\frac{I_F}{I_s} = e^{Vf/\eta V_T}$$

$$\therefore \quad \ln \frac{I_F}{I_s} = \frac{Vf}{\eta V_T} \quad \{\text{Taking log on both sides}\}$$

$$V_f = \eta V_T\ [\ln IF - \ln Is]$$

$$\therefore \quad V_f = \eta V_T \ln\left[\frac{I_F}{I_s}\right]$$

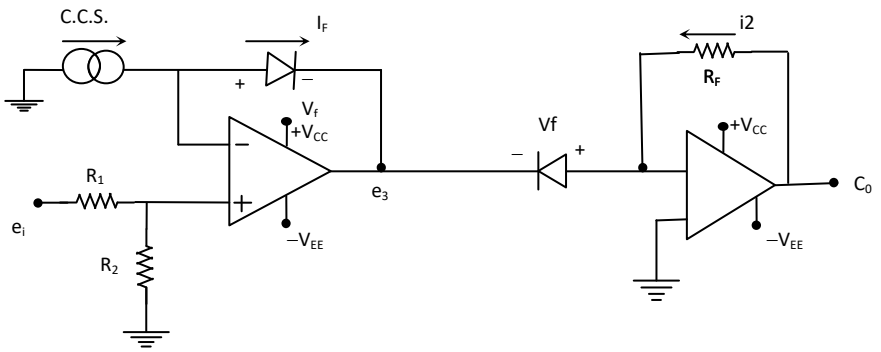
We know that,

$$-V_f = V_0 \qquad \& \qquad I_F = I = \frac{V_s}{R}$$

$$\therefore \quad V_0 = -\eta V_T\left[\ell n \frac{Vs}{R} - \ln.I_s\right]$$

Since V_0 is log of V_s, the circuit is working as log amplifier. Since I_s & V_T are temperature dependent V_0 varies with the temperature.

Antilog Amplifier :



$$e_2 = e_i . \frac{R_2}{R_1 + R_2}$$

$e_3 = e_{2-} V_f$

$= e_2 - \eta V_T [\ln I_F - \ln I_s]$ …(1)

Also $e_3 = -V_f$ {from A side}

$e_3 = -\eta V_T [\ln I_2 - \ln I_s]$ …(2)

equating (1) & (2) we get,

$e_2 - \eta V_T [\ln I_F - \ln I_s] = -\eta V_T [\ln I_2 - \ln I_s]$

$$e_2 = \eta V_T \ln \left[\frac{I_F}{I_2}\right] - \eta V_T \ln \frac{I_F R_F}{e_0}$$

because $I_2 = e_0/R_F$

$$ei . \frac{R_2}{R_1 + R_2} = \eta V_i \ln \frac{I_F R_F}{e_0}$$

$$\ln \left\{\frac{e_0}{I_F R_F}\right\} = -ei \left[\frac{R_2}{(R_1 + R_2)\eta V_{Tk}}\right]$$

$e_0 = I_F R_F \ln^{-1} (-ei . k)$

$\therefore e_0 = K_1 \ln^{-1} (-ei . k)$

o/P is antilog of ei, circuit works as antilog amplifier

Q.6(c) Write short note on Voltage Controlled Oscillator [V_{co}] **05**

Ans.: The V_{co} generates an o/p frequency that is directly proportional to its input voltage. A commonly available V_{co} is in IC form in signetics NE / SE 566.

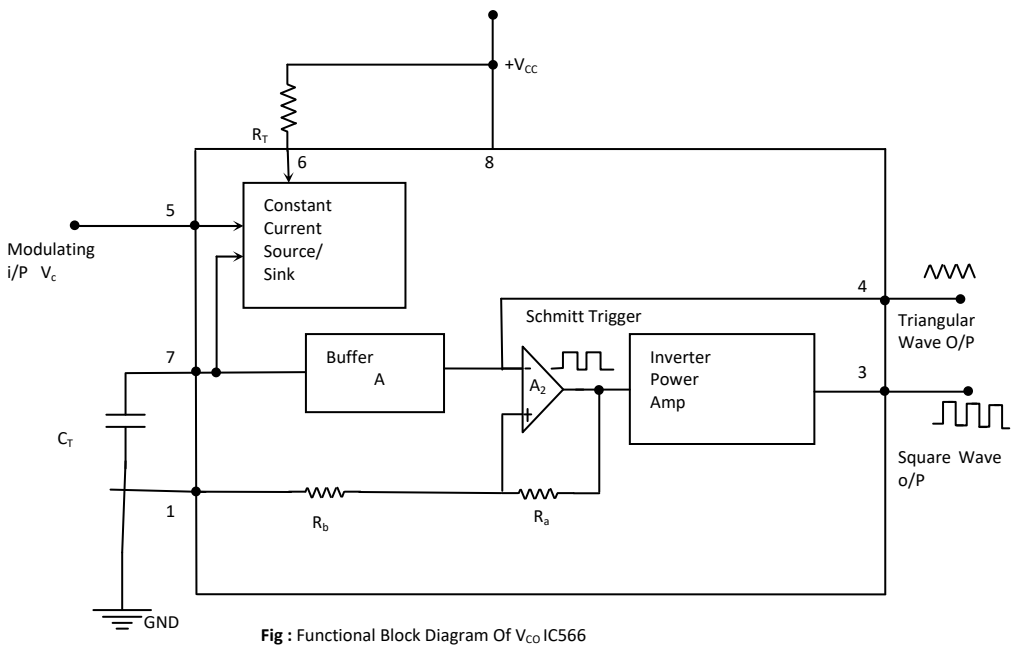


Fig : Functional Block Diagram Of V_{CO} IC566

→ The constant current source / sink block is used to charge or discharge the externally connected timing capacitor C_T linearly.

→ The value of charging & discharging current is dependent on the voltage V_c applied at pin no. 5 (modulating i/p).

→ This current can also be changed by changing the external timing resistor R_T.

→ The potential difference between pins (5) & (6) is almost zero. That means these pins are equipotential.

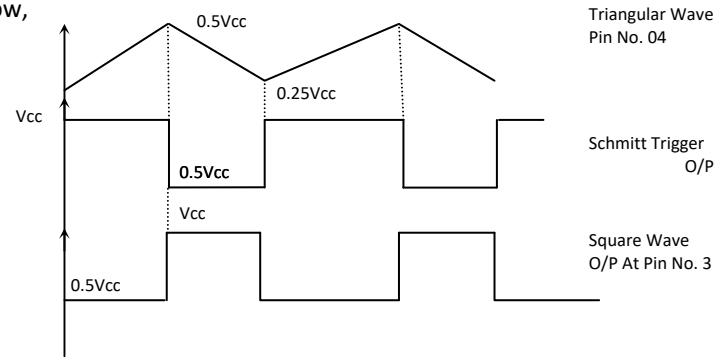
→ Therefore if we increase the modulating voltage V_c at pin. No. 5, then the voltage at pin no. 6 will increase with the same amount. This reduces the voltage drop across R_T & reduces the charging current

→ The voltage across capacitor is thus a triangular wave. This triangular wave is applied to Buffer A.

→ The Buffer avoids any possible loading of the Capacitor. The Buffer o/p is taken out at pin no (4) as a triangular wave o/p.

→ The Buffer is also applied to a Schmitt trigger A_2 which convers triangular wave into a square Waveform.

→ Resistors R_a & R_b provides upper & lower trigger voltages. These square wave is inverted by inverter A_3 & made available at pin no. 3. The o/p waveforms are as shown below,



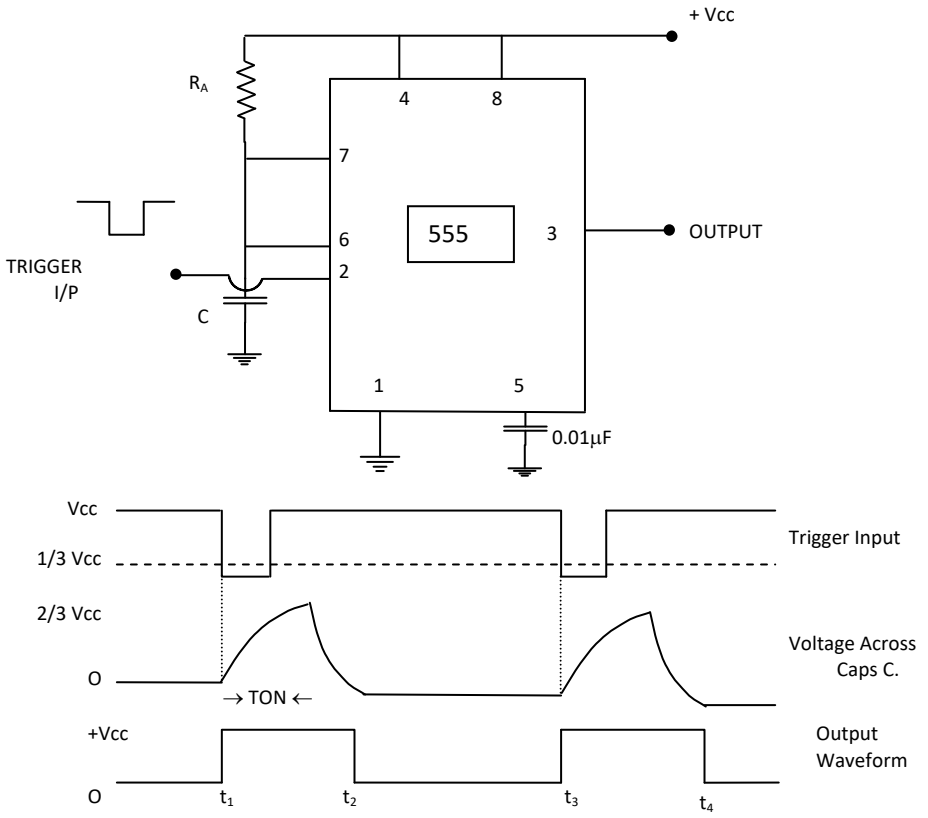
Output Waveform Of VCO IC566

→ The expression for o/p frequency is given by,

$$\left[f_0 = \frac{2(Vcc - Vc)}{R_T C_T Vcc} \right]_{11}$$

Q.6(d) Write short note on Monostable Multi-vibrator Using IC555. **05**

Ans.:



Interval (O to t_1)

→ In this interval, trigger i/p is held high at +vcc. The R.S. flip flop is initially set. ∴ Transistor T_1 is conducting & acts as a closed switch.

→ As the external capacitor C_1 is connected across T_1, it is bypassed & cannot charge & the voltage $V_c = 0$.

→ Therefore o/p voltage is O volts & flip flop is in "SET MODE".

Interval (t_1 to t_2)

→ At instant $t = t_2$, –ve going pulse is applied at the trigger i/p (pin no. 2).

→ As soon as trigger i/p voltage goes below $\frac{1}{3}$ Vcc, the o/p of lower comparator goes high.

→ This will reset SR flip flop, Q will become low & $\overline{Q}$ will be high. This T_1 will be turned OFF & o/p becomes high.

→ As T_1 is OFF, the capacitor C starts charging through the resistor R_A in an exponential manner.

→ The o/p will remain high from t_1 to t_2. This period is called as ON Time or T_{ON}.

Interval ($t = t_2$)

→ At instant $t = t_2$, Voltage on caps V_c = 2/3 Vcc. As soon as Vtg tries to cross 2/3 Vcc, the o/p of upper comparator will become high, This will set SR FlipFlop, So its o/p becomes high & $\overline{Q}$ becomes low.

→ Hence o/p vtg V_0 becomes low, T_1 is turned ON.

→ The Capacitor will discharge immediately through T_1

→ The o/p voltage remains low, till the next trigger pulse is applied. The low state of o/p is a stable state.

$T_{ON} = 1.1\ R_A.C$

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